

MODEL NAME : AAZ80

PCB NO : LA-C881P

BOM P/N : TBD



MS_PCB
DAA000AW000

	R1	R3	R3	R3
CPN	DAA000AW010	DAA000AW011	DAA000AW012	DAA000AW013

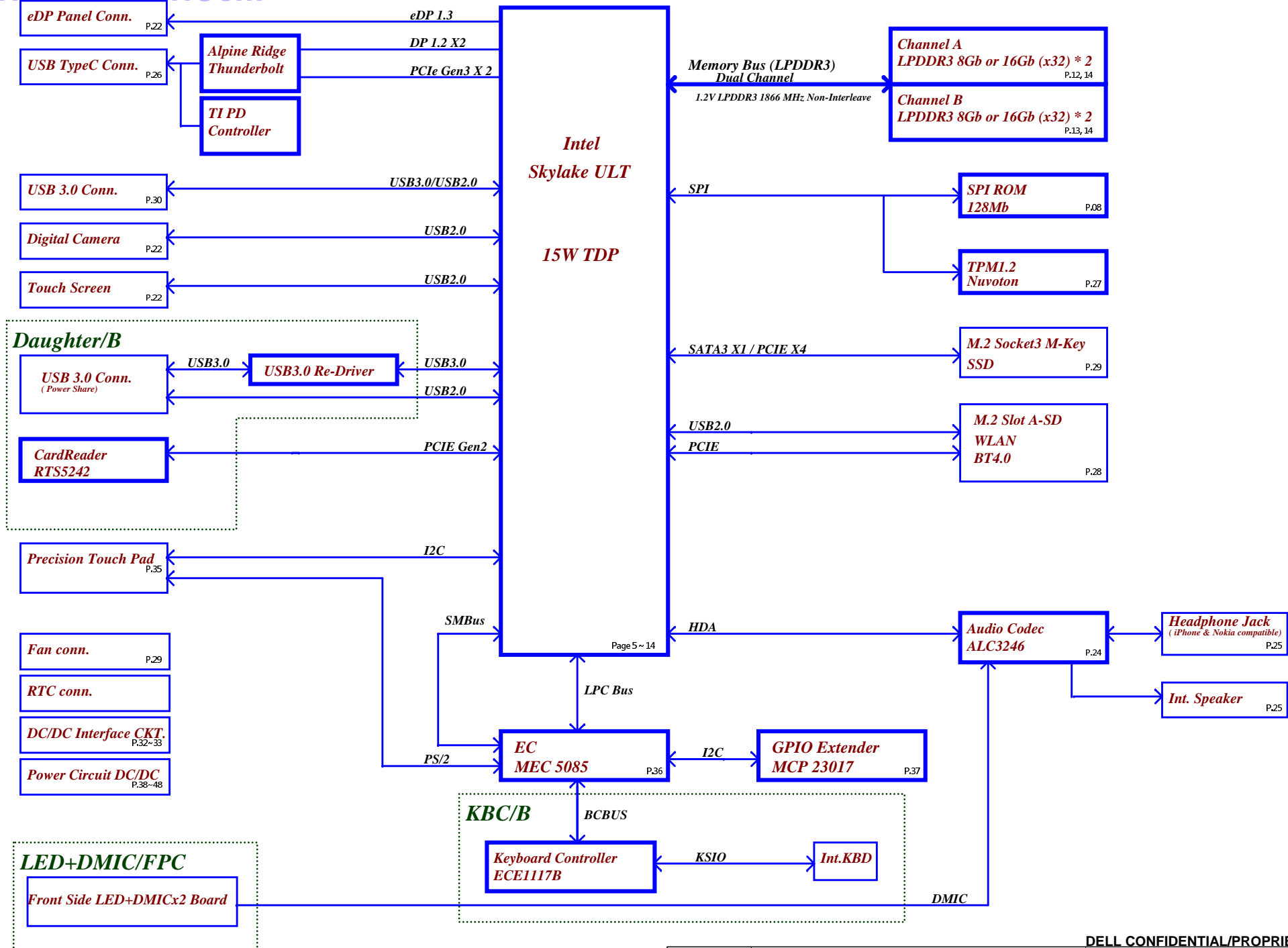
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Schematic Document

Dino2 (Skylake ULT)

2015-09-16

Rev: 1.0 (A00)



2+2 CPU Option

UCPU1 QJRK_2+2@ SA000090W1L FJ8066201931104 QJRK	UCPU1 QJRP_2+2@ SA000090C1L FJ8066201930408 QJRP	UCPU1 QJRM_2+2@ SA000090T1L FJ8066201924931 QJRM	UCPU1 QJRK_2+2@ SA000090P1L FJ8066201930408 QJRK	UCPU1 QJRH_2+2@ SA000090U1L FJ8066201924950 QJRH
UCPU1 SR2EU_2+2@ SA000090M1L FJ8066201931104 SR2EU	UCPU1 SR2EY_2+2@ SA000090C3L FJ8066201930408 SR2EY	UCPU1 SR2FO_2+2@ SA000090T3L FJ8066201924931 SR2FO	UCPU1 SR2EZ_2+2@ SA000090P3L FJ8066201930408 SR2EZ	UCPU1 SR2F1_2+2@ SA000090U3L FJ8066201924950 SR2F1

2+3 CPU Option

UCPU1 QK1Q_2+3@ SA000090C1L FJ8066202496511 QK1Q	UCPU1 QK2S_2+3@ SA000090E1L FJ8066202496507 QK2S
UCPU1 QK1P_2+3@ SA000090E1L FJ8066202496507 QK1P	UCPU1 QK2Q_2+3@ SA000090E1L FJ8066202496508 QK2Q

AR Option

UT1 AR_OSIN@ SA000090W1L DSL6340 QJIN B1
UT1 AR_SLL42@ SA000090N1L DSL6340 SLL42 B1

DRAM Option

Micron 4G/1866	UD19 MAG_1866@ SA00008PF1L EDF8132A3MA-JD-F-R A311	UD20 MAG_1866@ SA00008PF1L EDF8132A3MA-JD-F-R A311	UD21 MAG_1866@ SA00008PF1L EDF8132A3MA-JD-F-R A311	UD22 MAG_1866@ SA00008PF1L EDF8132A3MA-JD-F-R A311	MEM_CONFIG0 RH144 MAG_1866@ SD028100280 10K_0402_5%	MEM_CONFIG1 RH139 MAG_1866@ SD028100280 10K_0402_5%	MEM_CONFIG2 RH145 MAG_1866@ SD028100280 10K_0402_5%	MEM_CONFIG3 RH151 MAG_1866@ SD028100280 10K_0402_5%	MEM_CONFIG4 RH147 MAG_1866@ SD028100280 10K_0402_5%
Micron 8G/1866	UD19 MBG_1866@ SA00008Q11L EDFA232A2MA-JD-F-R A311	UD20 MBG_1866@ SA00008Q11L EDFA232A2MA-JD-F-R A311	UD21 MBG_1866@ SA00008Q11L EDFA232A2MA-JD-F-R A311	UD22 MBG_1866@ SA00008Q11L EDFA232A2MA-JD-F-R A311	RH129 MBG_1866@ SD028100280 10K_0402_5%	RH150 MBG_1866@ SD028100280 10K_0402_5%	RH149 MBG_1866@ SD028100280 10K_0402_5%	RH151 MBG_1866@ SD028100280 10K_0402_5%	RH147 MBG_1866@ SD028100280 10K_0402_5%
Hynix 4G/1866	UD19 HMG_1866@ SA00008G61L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD20 HMG_1866@ SA00008G61L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD21 HMG_1866@ SA00008G61L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD22 HMG_1866@ SA00008G61L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	RH129 HMG_1866@ SD028100280 10K_0402_5%-D	RH139 HMG_1866@ SD028100280 10K_0402_5%-D	RH149 HMG_1866@ SD028100280 10K_0402_5%-D	RH151 HMG_1866@ SD028100280 10K_0402_5%-D	RH147 HMG_1866@ SD028100280 10K_0402_5%-D
Hynix 8G/1866	UD19 HBG_1866@ SA00008FJ1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD20 HBG_1866@ SA00008FJ1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD21 HBG_1866@ SA00008FJ1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD22 HBG_1866@ SA00008FJ1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	RH144 HBG_1866@ SD028100280 10K_0402_5%-D	RH139 HBG_1866@ SD028100280 10K_0402_5%-D	RH149 HBG_1866@ SD028100280 10K_0402_5%-D	RH151 HBG_1866@ SD028100280 10K_0402_5%-D	RH147 HBG_1866@ SD028100280 10K_0402_5%-D
Samsung 4G/1866	UD19 S4G_1866@ SA00008PO1L K4EB304EE-EGCF A311	UD20 S4G_1866@ SA00008PO1L K4EB304EE-EGCF A311	UD21 S4G_1866@ SA00008PO1L K4EB304EE-EGCF A311	UD22 S4G_1866@ SA00008PO1L K4EB304EE-EGCF A311	RH144 S4G_1866@ SD028100280 10K_0402_5%-D	RH150 S4G_1866@ SD028100280 10K_0402_5%-D	RH149 S4G_1866@ SD028100280 10K_0402_5%-D	RH151 S4G_1866@ SD028100280 10K_0402_5%-D	RH147 S4G_1866@ SD028100280 10K_0402_5%-D
Samsung 8G/1866	UD19 S8G_1866@ SA00008QV1L K4EB304EE-EGCF A311	UD20 S8G_1866@ SA00008QV1L K4EB304EE-EGCF A311	UD21 S8G_1866@ SA00008QV1L K4EB304EE-EGCF A311	UD22 S8G_1866@ SA00008QV1L K4EB304EE-EGCF A311	RH129 S8G_1866@ SD028100280 10K_0402_5%-D	RH139 S8G_1866@ SD028100280 10K_0402_5%-D	RH145 S8G_1866@ SD028100280 10K_0402_5%-D	RH146 S8G_1866@ SD028100280 10K_0402_5%-D	RH152 S8G_1866@ SD028100280 10K_0402_5%-D
Micron 16G/1866	UD19 M16G_1866@ SA00008QW1L EDFB232A1MA-JD-F-R A311	UD20 M16G_1866@ SA00008QW1L EDFB232A1MA-JD-F-R A311	UD21 M16G_1866@ SA00008QW1L EDFB232A1MA-JD-F-R A311	UD22 M16G_1866@ SA00008QW1L EDFB232A1MA-JD-F-R A311	RH144 M16G_1866@ SD028100280 10K_0402_5%-D	RH150 M16G_1866@ SD028100280 10K_0402_5%-D	RH145 M16G_1866@ SD028100280 10K_0402_5%-D	RH151 M16G_1866@ SD028100280 10K_0402_5%-D	RH147 M16G_1866@ SD028100280 10K_0402_5%-D
Samsung 16G/2133	UD19 S16G_2133@ SA00008VV1L K4EB304EB-EGCG A311	UD20 S16G_2133@ SA00008VV1L K4EB304EB-EGCG A311	UD21 S16G_2133@ SA00008VV1L K4EB304EB-EGCG A311	UD22 S16G_2133@ SA00008VV1L K4EB304EB-EGCG A311	RH129 S16G_2133@ SD028100280 10K_0402_5%-D	RH150 S16G_2133@ SD028100280 10K_0402_5%-D	RH145 S16G_2133@ SD028100280 10K_0402_5%-D	RH151 S16G_2133@ SD028100280 10K_0402_5%-D	RH152 S16G_2133@ SD028100280 10K_0402_5%-D
Samsung 16G/1866	UD19 S16G_1866@ SA00008X11L K4EB304EB-EGCF A311	UD20 S16G_1866@ SA00008X11L K4EB304EB-EGCF A311	UD21 S16G_1866@ SA00008X11L K4EB304EB-EGCF A311	UD22 S16G_1866@ SA00008X11L K4EB304EB-EGCF A311	RH144 S16G_1866@ SD028100280 10K_0402_5%-D	RH139 S16G_1866@ SD028100280 10K_0402_5%-D	RH145 S16G_1866@ SD028100280 10K_0402_5%-D	RH146 S16G_1866@ SD028100280 10K_0402_5%-D	RH152 S16G_1866@ SD028100280 10K_0402_5%-D
Hynix 16G/1866	UD19 H16G_1866@ SA00008YT1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD20 H16G_1866@ SA00008YT1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD21 H16G_1866@ SA00008YT1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	UD22 H16G_1866@ SA00008YT1L H5CCNNHGTMLAR-NUD AB8CCNNHGTMLAR-NUD A311	RH129 H16G_1866@ SD028100280 10K_0402_5%-D	RH150 H16G_1866@ SD028100280 10K_0402_5%-D	RH149 H16G_1866@ SD028100280 10K_0402_5%-D	RH151 H16G_1866@ SD028100280 10K_0402_5%-D	RH147 H16G_1866@ SD028100280 10K_0402_5%-D

Board ID Table for AD channel

RE79	CE54	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

	SKU	PTT	TPM2.0
Dino2	Vpro+CS	Disable	Enable
	nVpro+CS	Enable	None

SMBUS Control Table

	SOURCE	23017	BATTERY	Charger	PD	5085	XDP	Audio	Touch Pad
I2C1A_CLK I2C1A_DATA	MEC5085	V							
I2C1C_CLK I2C1C_DATA	MEC5085		V						
I2C1G_CLK I2C1G_DATA	MEC5085			V					
I2C2A_CLK I2C2A_DATA	MEC5085				V				
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH					V			
SMBCLK SMBDATA	PCH						V		
I2C0_CLK I2C0_DATA	PCH								
I2C1_CLK I2C1_DATA	PCH								V

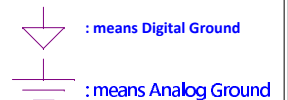
PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	External USB3(On IOB)
	2	External USB3(On MB)
	3	NGFF CARD WLAN
	4	Touch Panel
	5	Camera
	6	
	7	
PCH USB 3.0 Port Mapping	1	External USB3(On IOB)
	2	External USB3(On MB)

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Alpine Ridge
	CLKOUT_PCIE1	NGFF CARD WLAN	Lane 2	Alpine Ridge
	CLKOUT_PCIE2		Lane 3	
	CLKOUT_PCIE3	M.2 SSD / PCIe	Lane 4	
	CLKOUT_PCIE4		Lane 5	NGFF CARD WLAN
	CLKOUT_PCIE5	Card Reader	Lane 6	Card Reader
	FLEX CLK#	DESTINATION	Lane 7	
	CLKOUT_LPC_0	EC LPC	Lane 8	
	CLKOUT_LPC_1	Debug	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

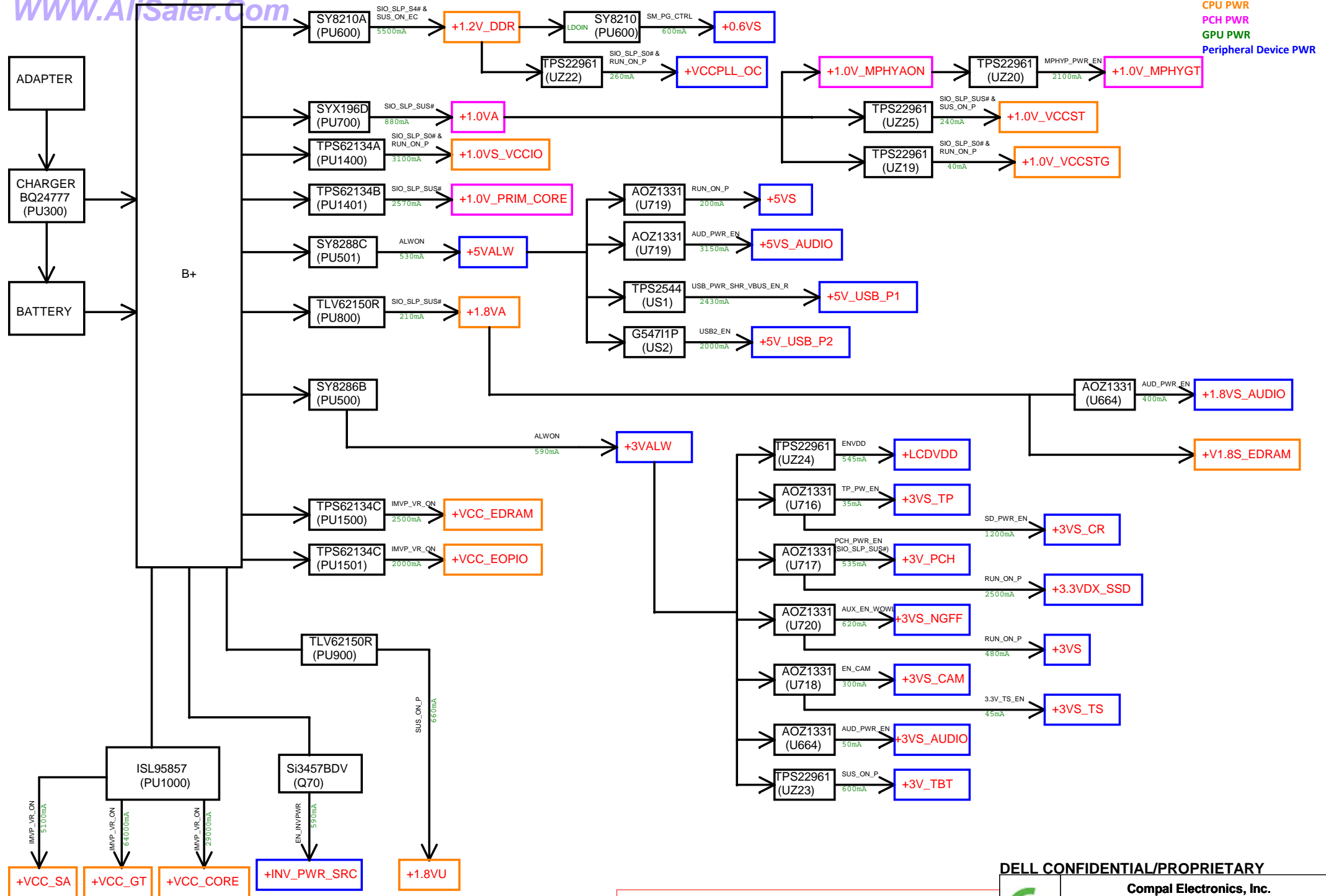
SATA PORT#	DESTINATION
SATA-0	
SATA-1A	
SATA-1B	
SATA-2	M.2 SSD

Symbol Note :



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Security Classification		Compal Secret Data		Title	
Issued Date	2013/07/04	Deciphered Date	2013/10/28	P04-Notes List	
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Compal Electronics, Inc.

P05-Power rails

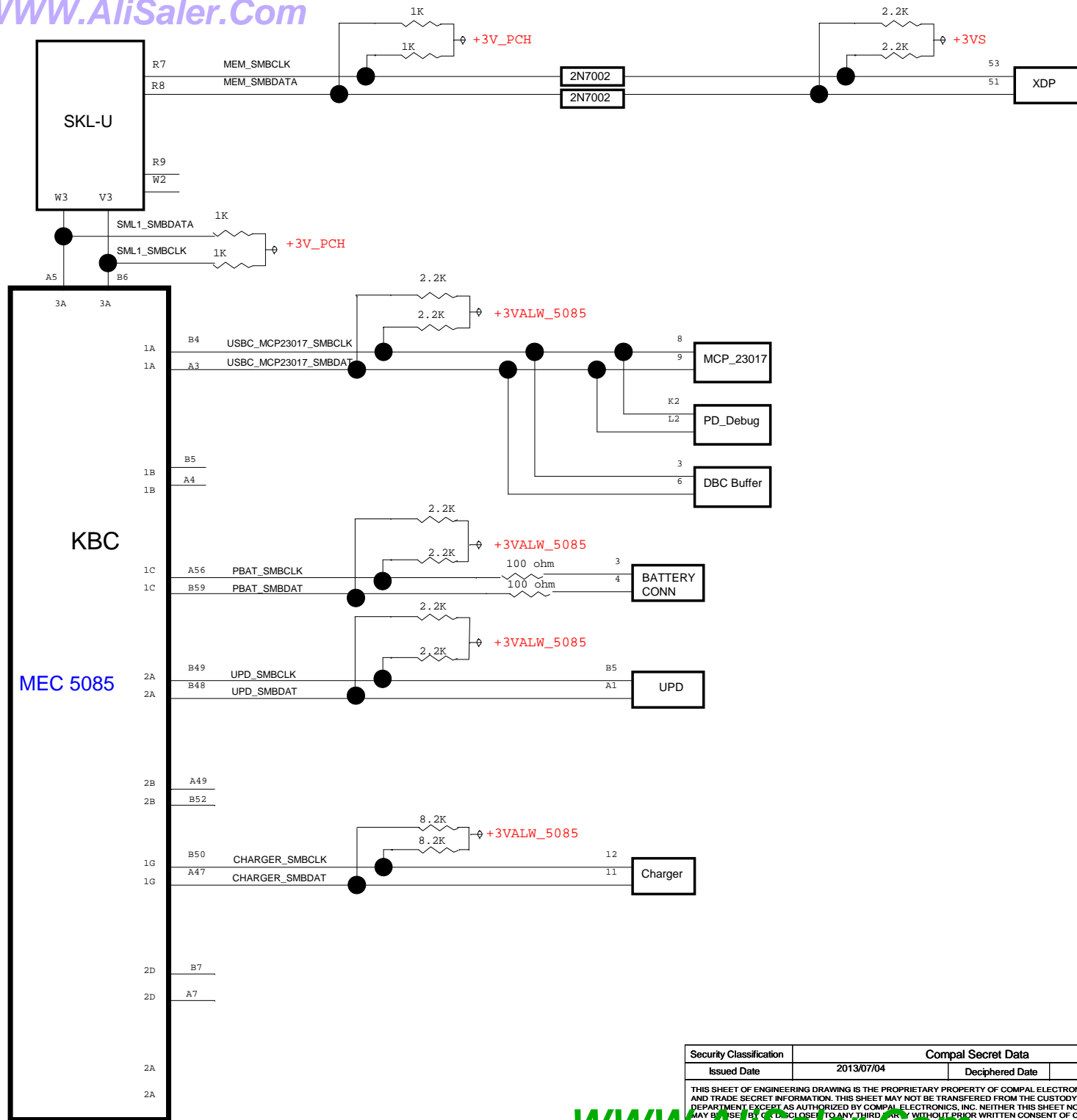
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LA-C661F

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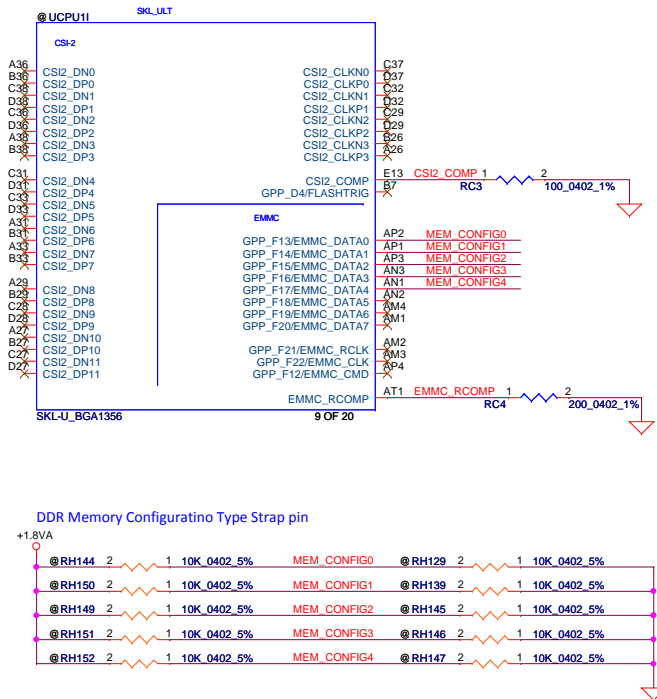
Compal Electronics, Inc.

Security Classification
Issued Date
2013/07/04
Deciphered Date
2013/10/28

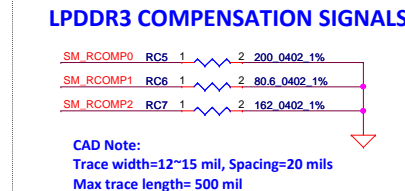
Title
P06-SMBus block diagram

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LA-C881P
Rev
1.0
Date: Tuesday, October 13, 2015
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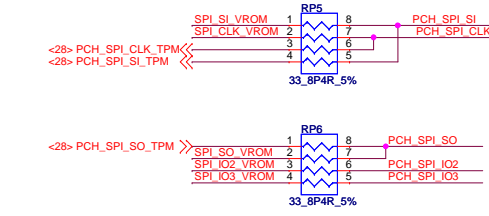
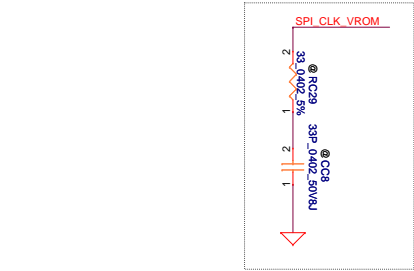
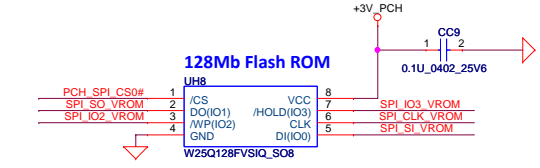
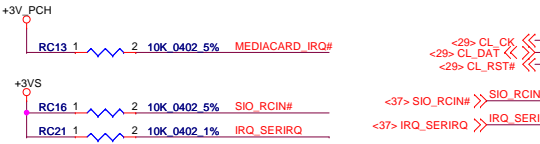
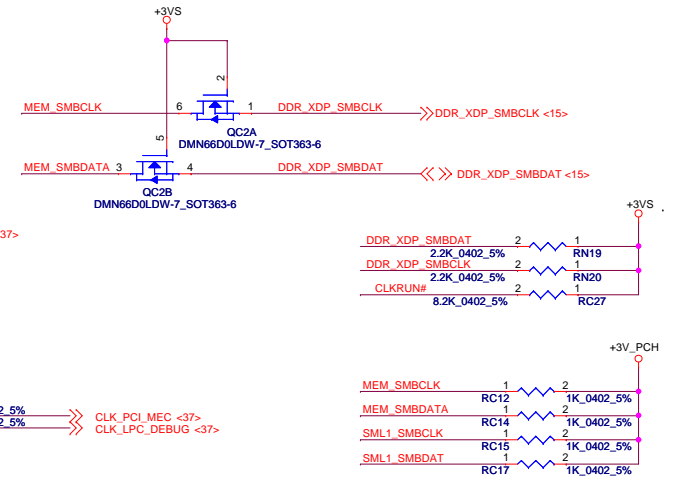
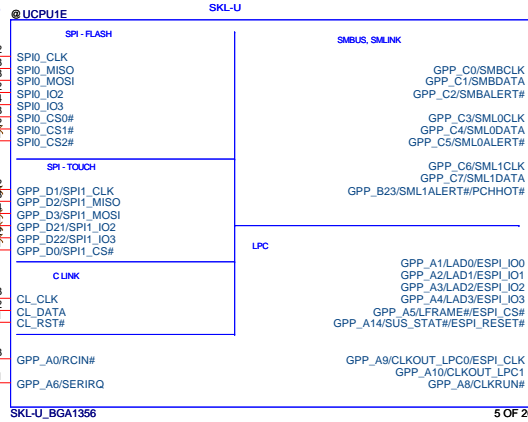


GPIO Pin	Pin Name	1600 Mbps	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0		0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1		0	0	1	1	0	0	1	1	0
GPP_D7	MEM_CONFIG2		0	0	0	0	1	1	1	1	0
GPP_D8	MEM_CONFIG3		0	0	0	0	0	0	0	0	1
GPP_D9	MEM_CONFIG4		0	0	0	0	0	0	0	0	0
GPIO Pin	Pin Name	1866 Mbps	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0		1	0	1	0	1	0	1	0	1
GPP_D6	MEM_CONFIG1		0	1	1	0	0	1	1	0	0
GPP_D7	MEM_CONFIG2		0	0	0	1	1	1	1	0	0
GPP_D8	MEM_CONFIG3		1	1	1	1	1	1	1	0	0
GPP_D9	MEM_CONFIG4		0	0	0	0	0	0	0	0	1
GPIO Pin	Pin Name	2133 Mbps	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0		0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_D7	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_D8	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_D9	MEM_CONFIG4		1	1	1	1	1	1	1	1	1



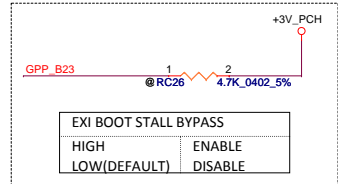
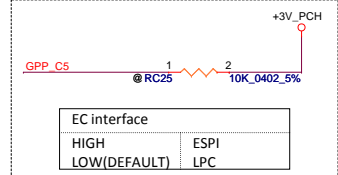
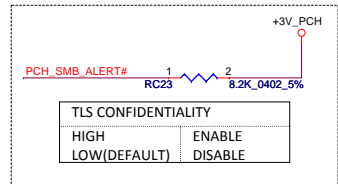
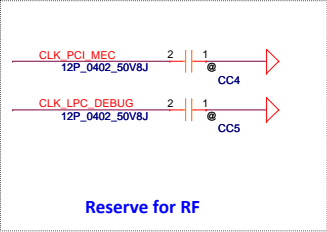
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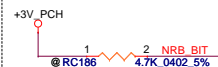
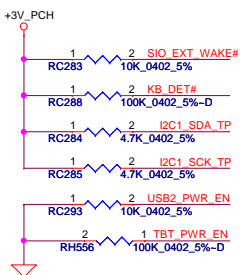
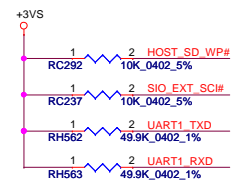
SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH_EDS R0.7 p.235~236



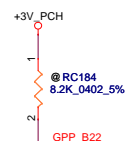
9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor(MOW WW5).
In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES- and SKL S/H platforms with pre-ES1/ES1 samples(MOW WW9).

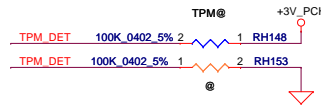
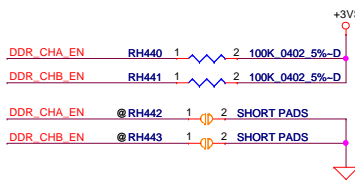
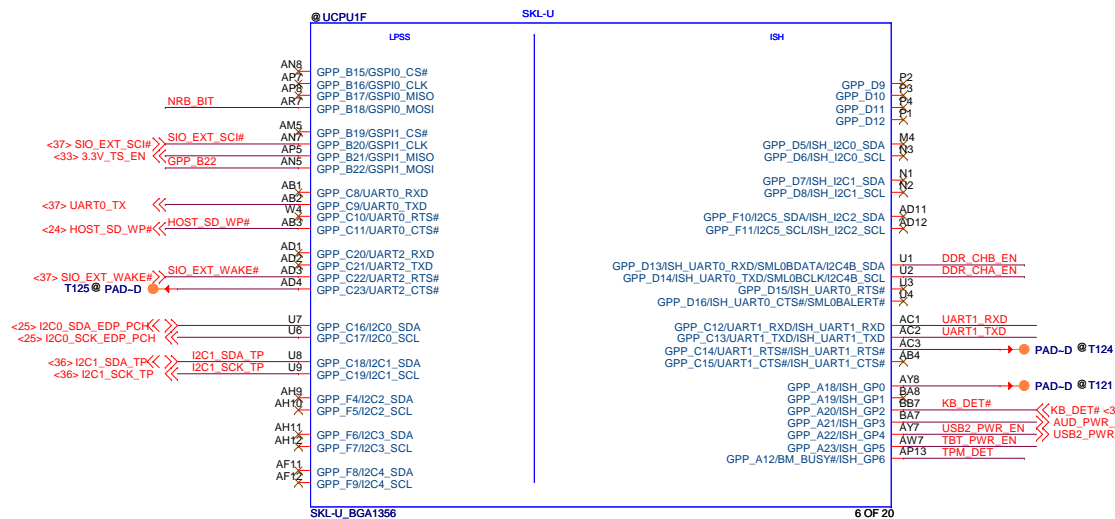




NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE
Weak IPD	

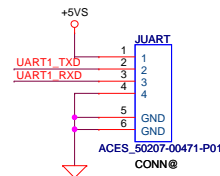


BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI



TPM BOM Optional

TPM_DET	
TPM	1 = W/TPM
	0 = W/O TPM

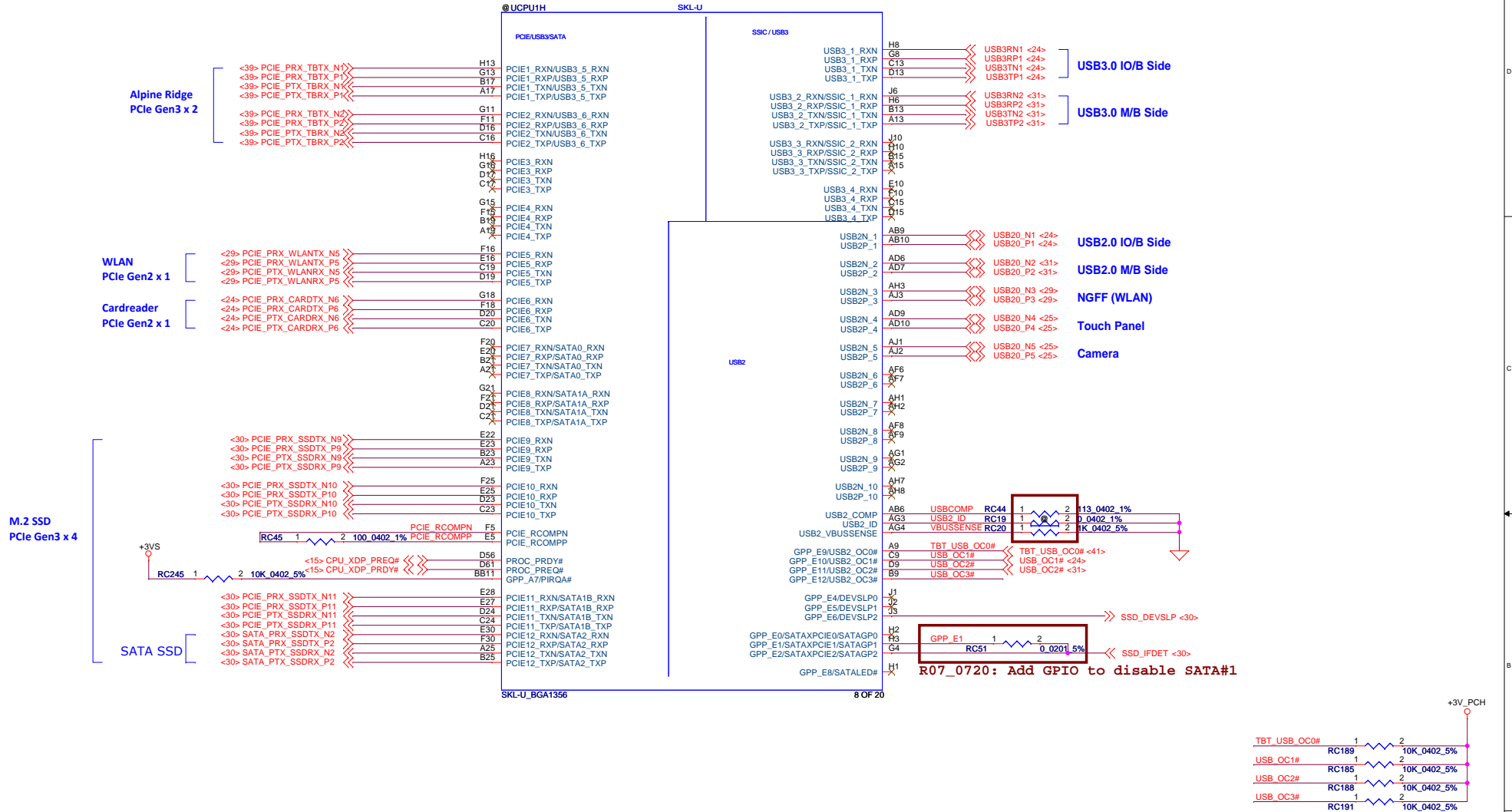


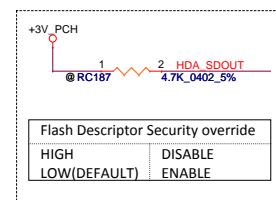
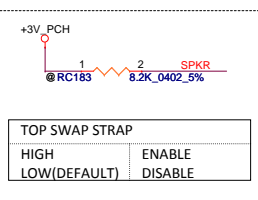
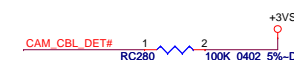
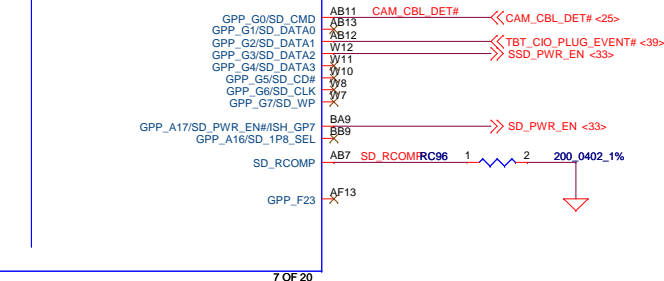
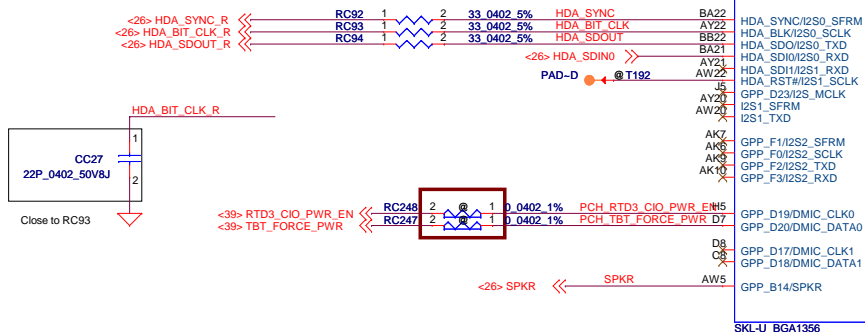
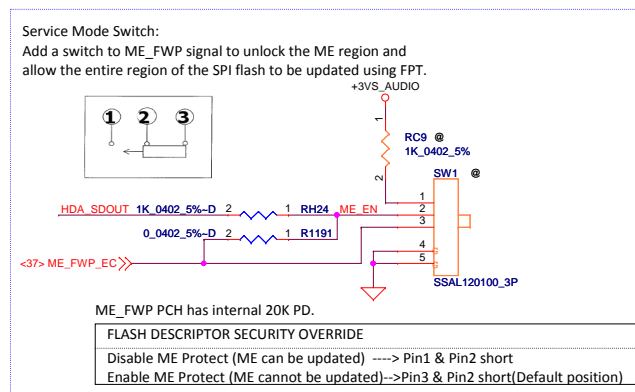
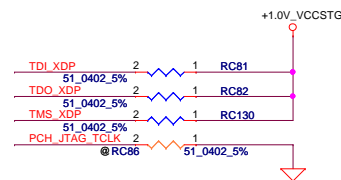
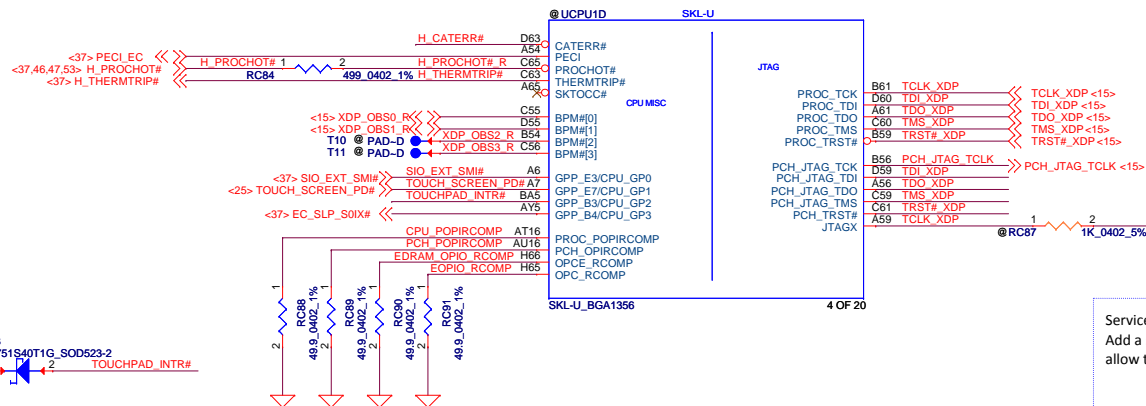
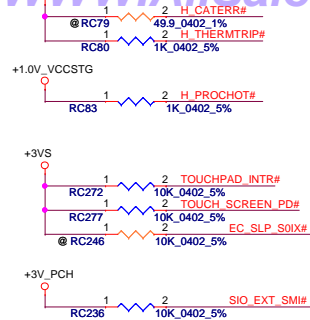
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

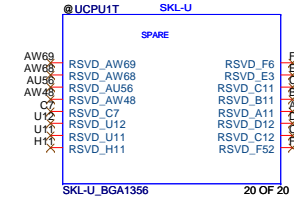
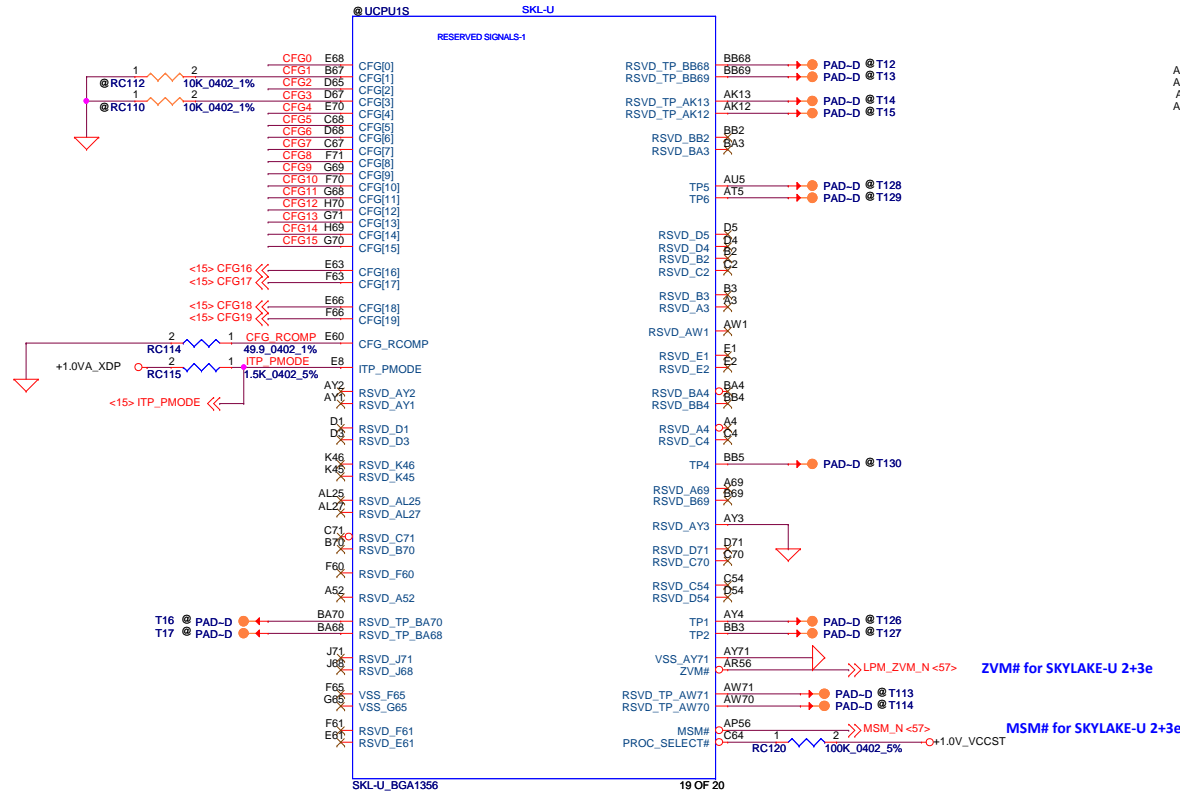
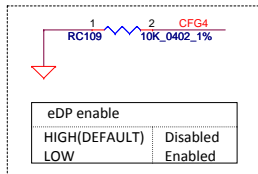
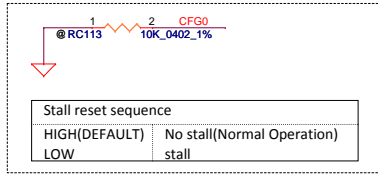
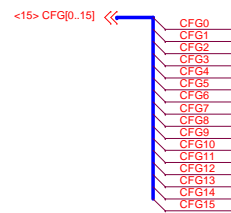
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Issued Date	2013/07/04	Deciphered Date
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Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title	P13-MCP(7/14)MISC,JTAG,HDA,SDIO
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PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:

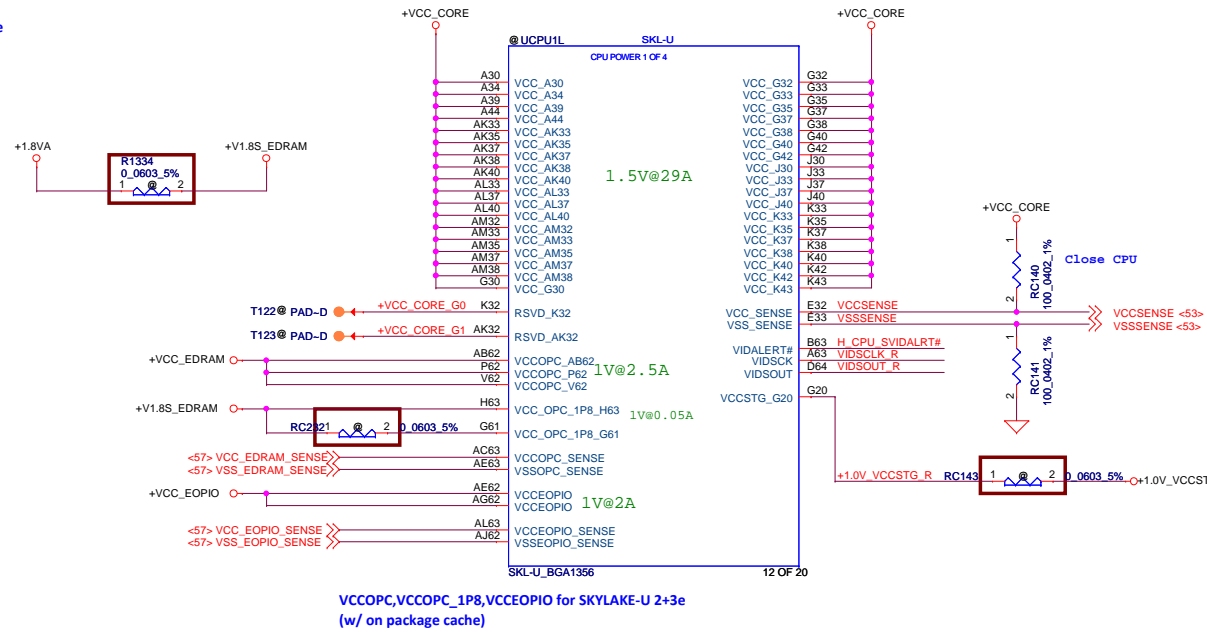
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.55~1.5V, 29A

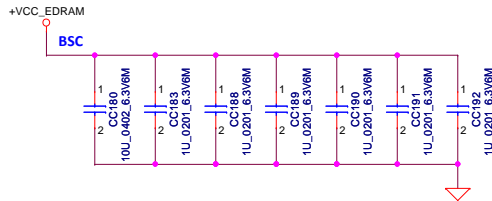
+VCC_EDRAM: 1V, 2.5A

+V1.8S_EDRAM: 1.8V, 50mA

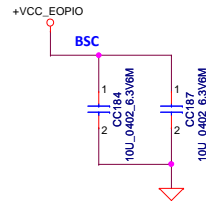
+VCC_EOPIO: 0.8~1V, 2A



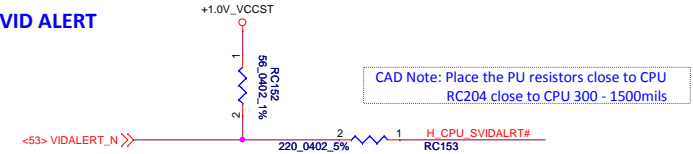
+VCC_EDRAM Decoupling Requirement
Back Side (underneath the package):
10U_0402*1 pcs + 1U_0201*6 pcs



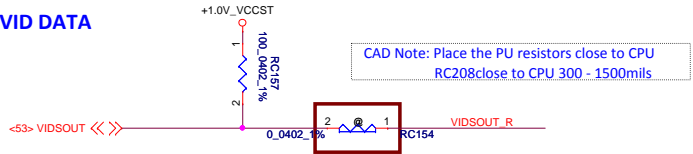
+VCC_EOPIO Decoupling Requirement
Back Side (underneath the package):
10U_0402*2 pcs



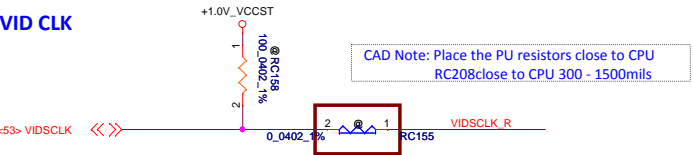
SVID ALERT



SVID DATA

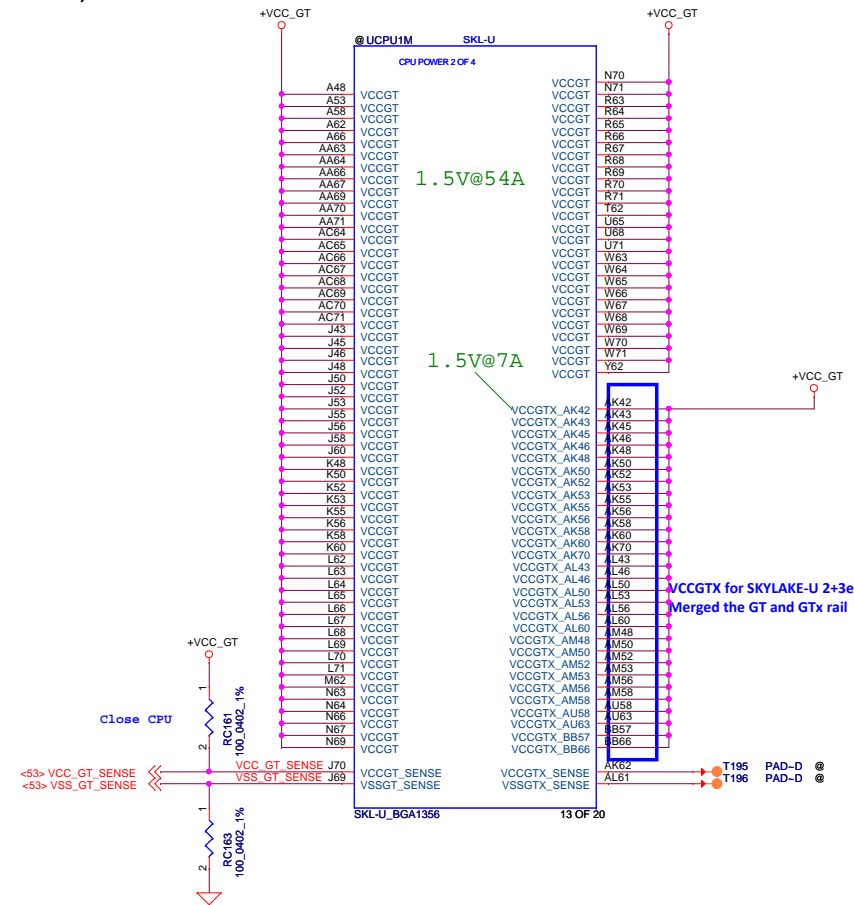


SVID CLK



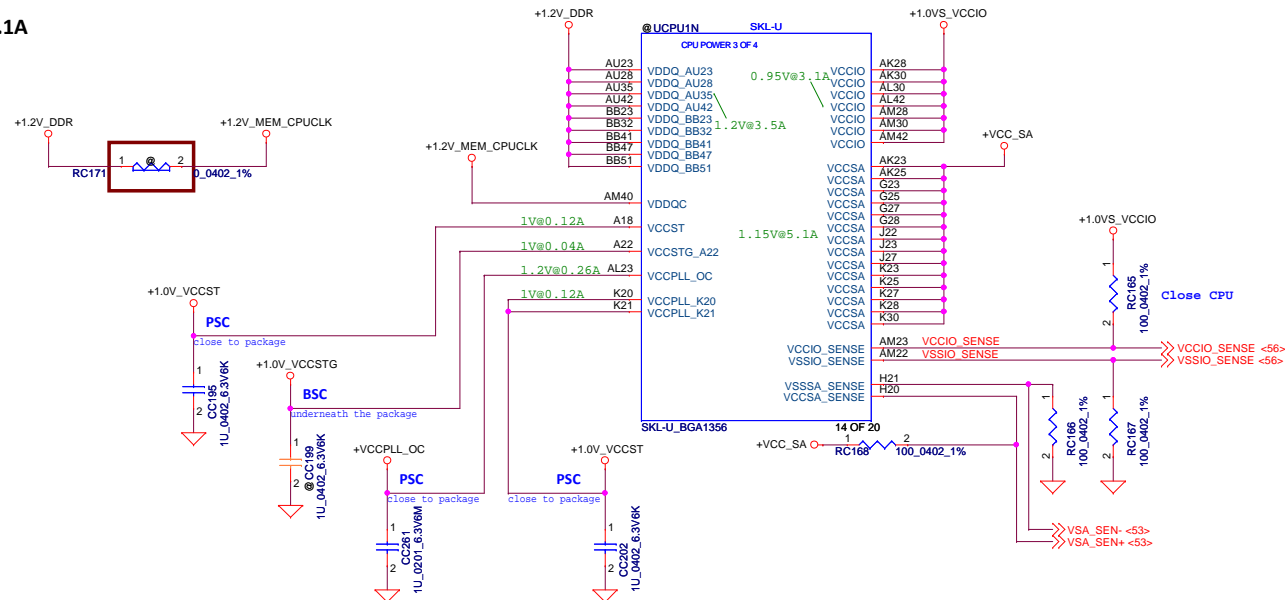
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Issued Date				2013/07/04				Compal Electronics, Inc.			
Deciphered Date				2013/10/28				P16-MCP(10/14)PWR-VCC CORE			
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+VCCGT: 0.55~1.5V, 54A
+VCCGTx: 0.55~1.5V, 7A

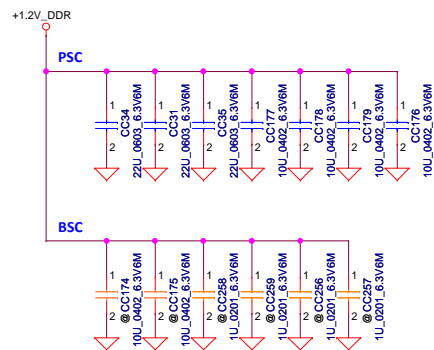


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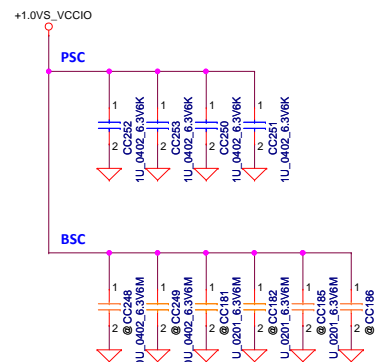
+1.2V_DDR: 1.2V, 3.5A
 +1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
 +1.0V_VCCSTG: 1V, 40mA
 +VCCPLL_OC: 1.2V, 260mA
 +1.0VS_VCCIO: 0.85~0.95V, 3.1A
 +VCC_SA: 1.15V, 5.1A



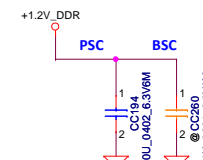
+1.2V_DDR Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (●)
 Primary Side (close to package):
 10U_0402*4 pcs + 22U_0603*3 pcs



+1.0VS_VCCIO Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (●)
 Primary Side (close to package):
 1U_0402*4 pcs



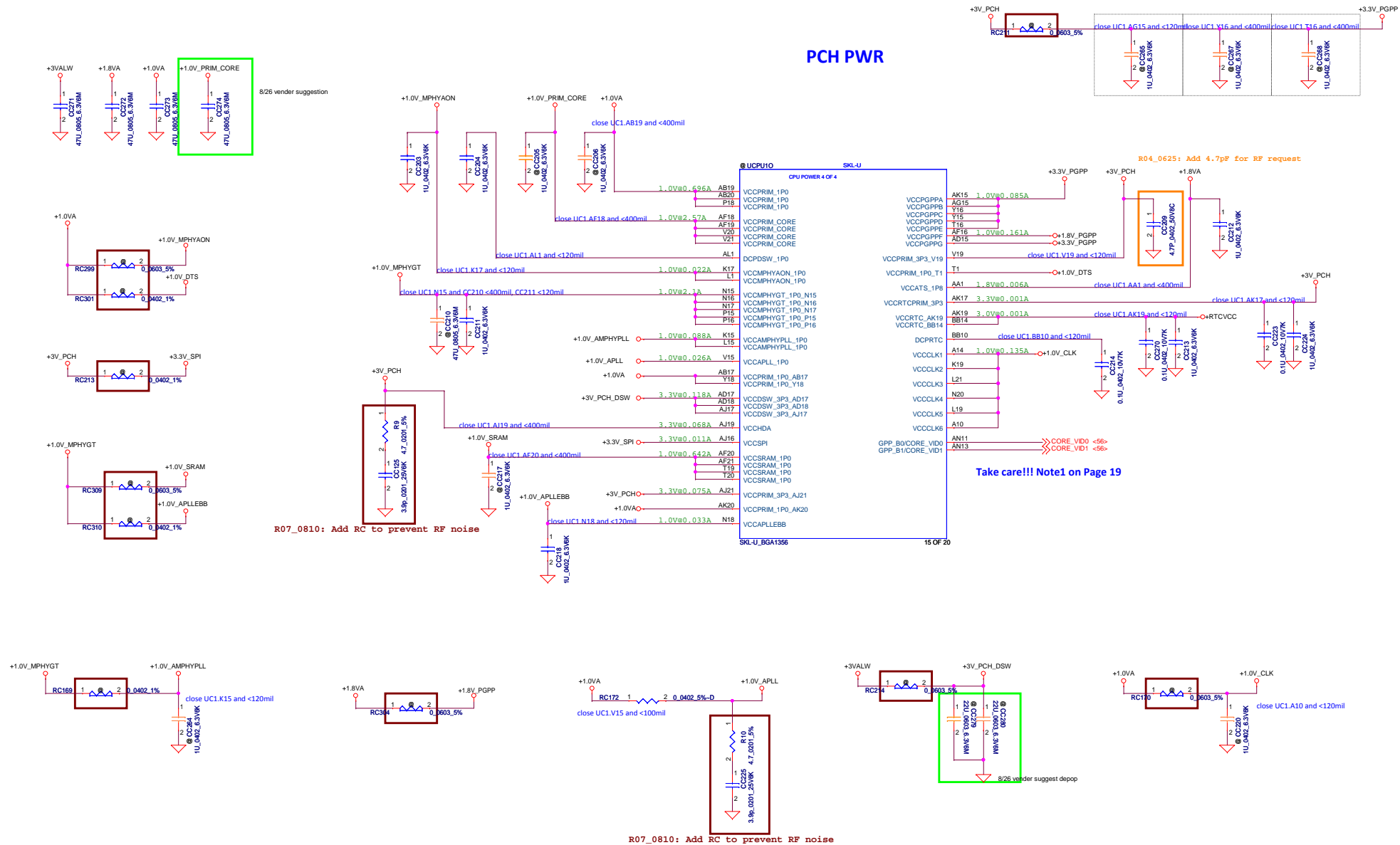
+1.2V_MEM_CPUCCLK (VDDQC) Place on CPU
 Back Side (underneath the package):
 1U_0201*1 pcs (●)
 Primary Side (close to package):
 10U_0402 * 1 pcs



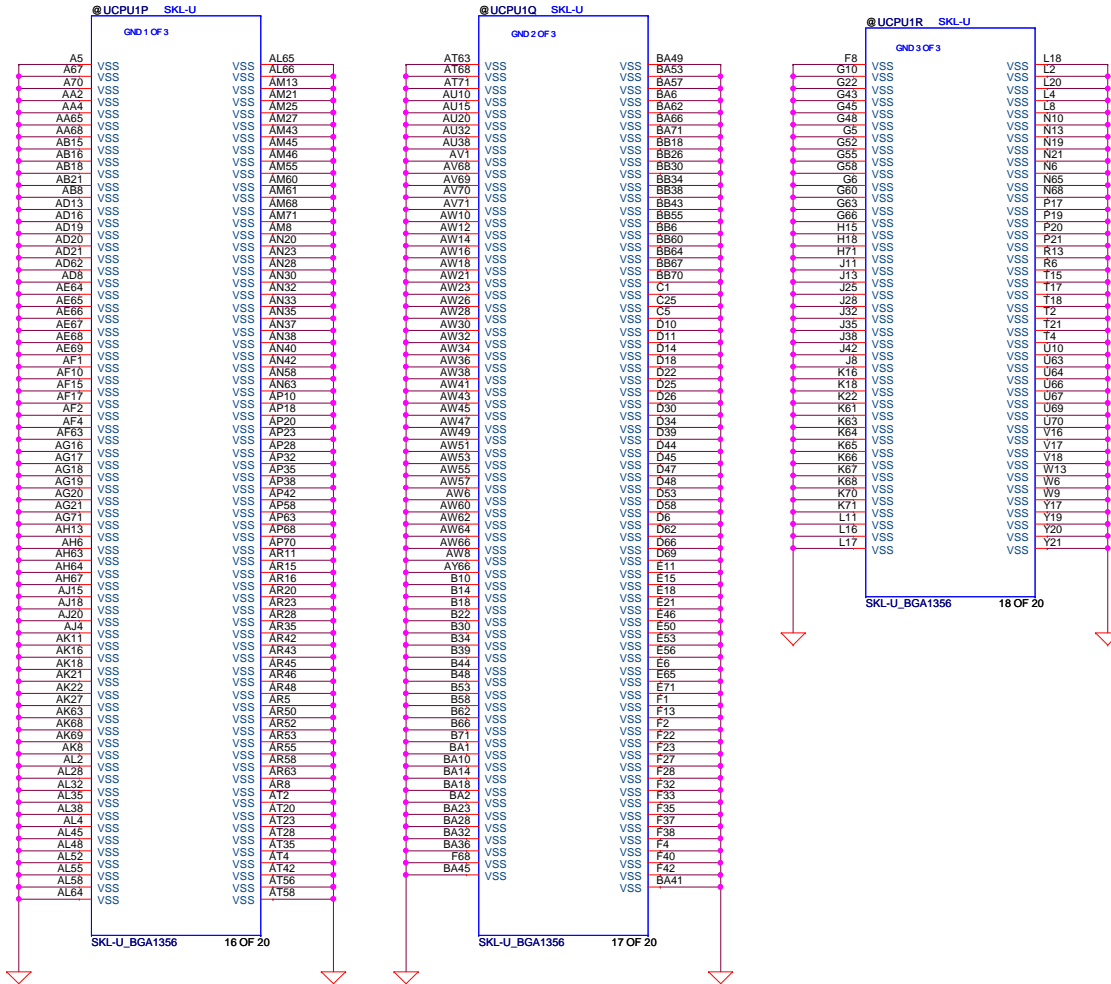
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Deciphered Date				2013/10/28		P19-MCP(13/14)PCH PWR	
Title				Document Number		LA-C881P	
Size				Revision		1.0	
Date				Tuesday, October 13, 2015		Sheet 19 of 59	

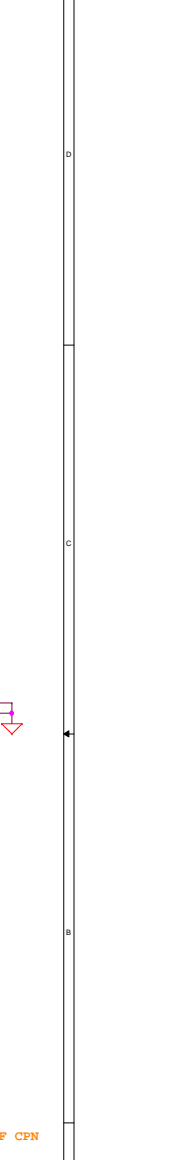
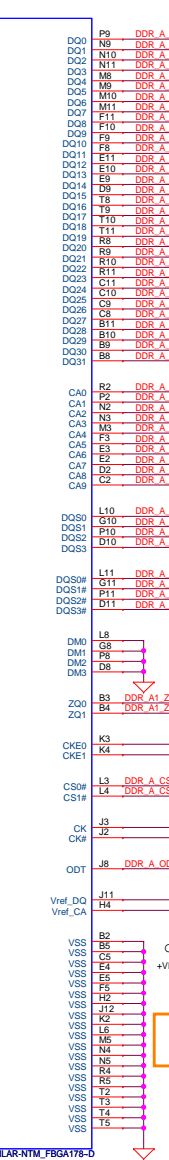
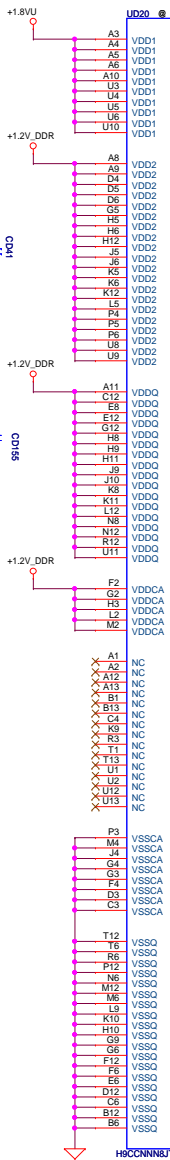
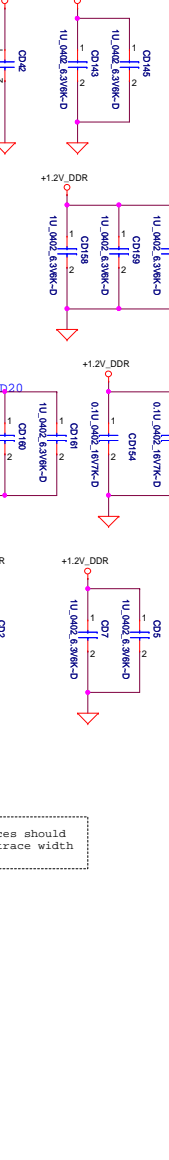
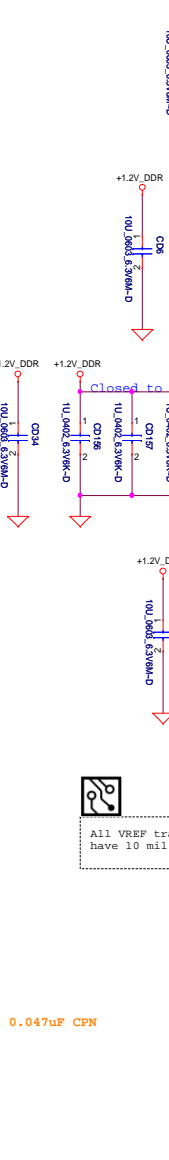
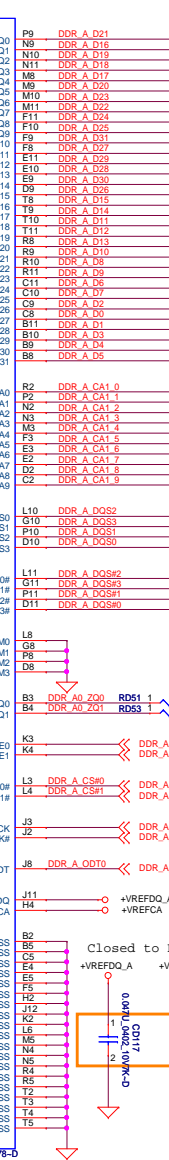
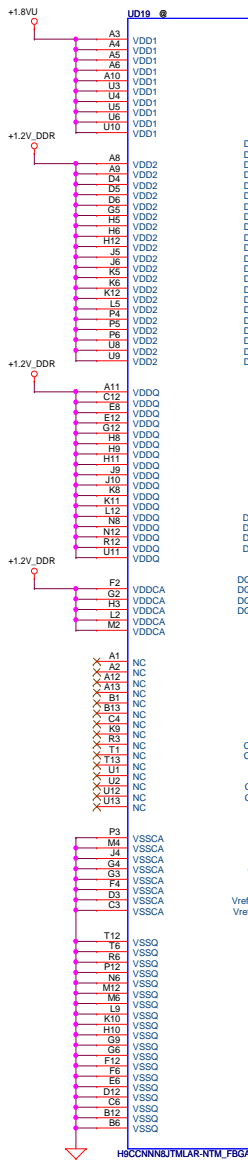
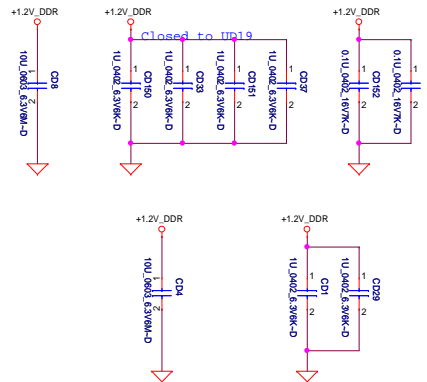
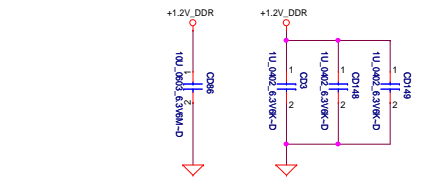


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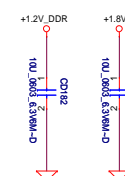
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<8> DDR_A_DQS#[0..7]
 <8> DDR_A_DQS#[0..7]
 <8> DDR_A_DQ[0..63]
 <23.8> DDR_A_CA1_[0..9]
 <23.8> DDR_A_CA2_[0..9]

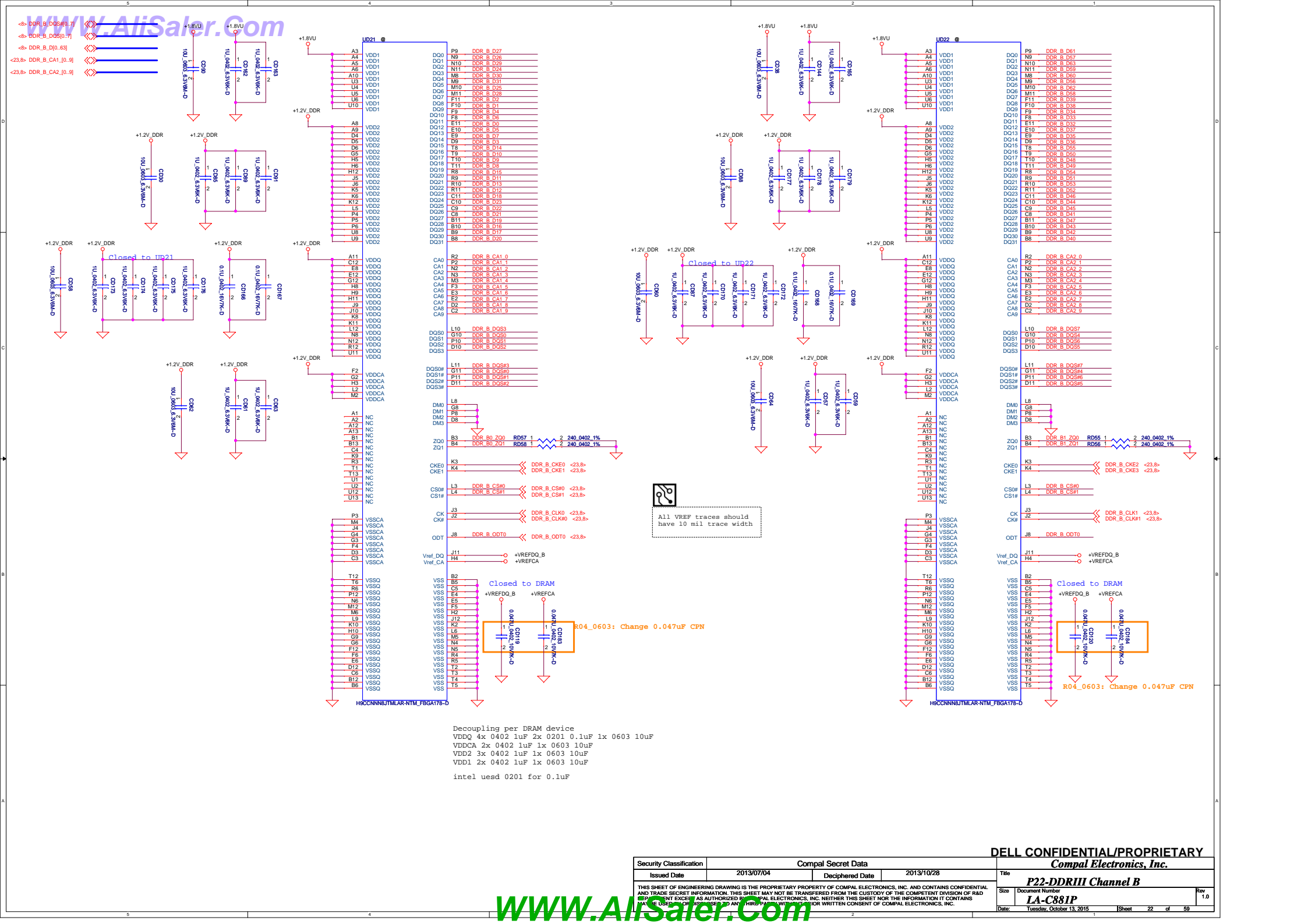


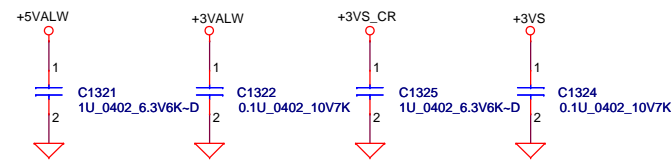
Decoupling per DRAM device
 VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF
 VDDCA 2x 0402 1uF 1x 0603 10uF
 VDD2 3x 0402 1uF 1x 0603 10uF
 VDD1 2x 0402 1uF 1x 0603 10uF
 intel used 0201 for 0.1uF



All VREF traces should have 10 mil trace width

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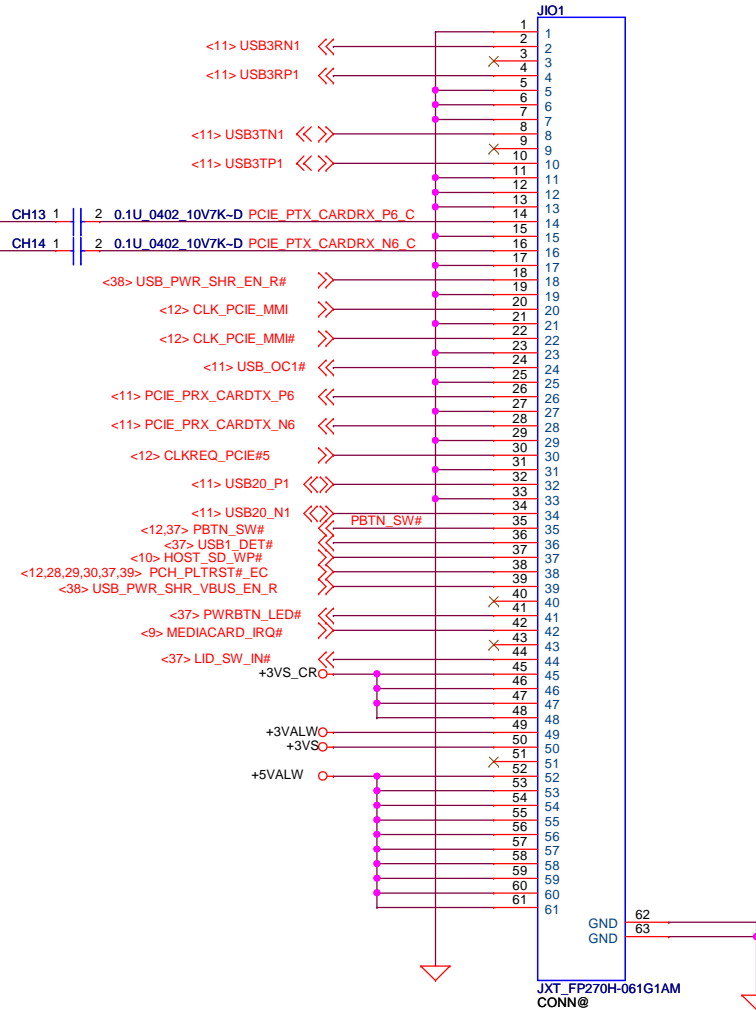
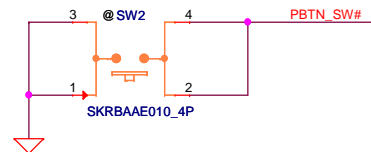




<11> PCIE_PTX_CARDRX_P6
<11> PCIE_PTX_CARDRX_N6

CH13 1 2 0.1U_0402_10V7K-D PCIE_PTX_CARDRX_P6 C
CH14 1 2 0.1U_0402_10V7K-D PCIE_PTX_CARDRX_N6 C

NPI Stage Power Switch

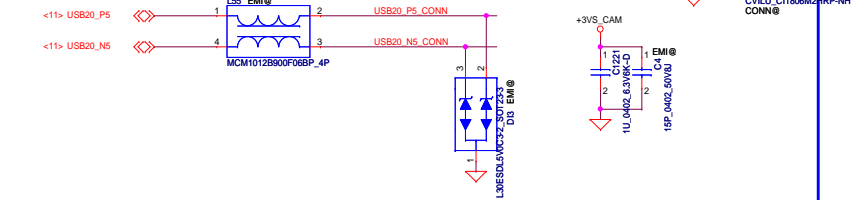


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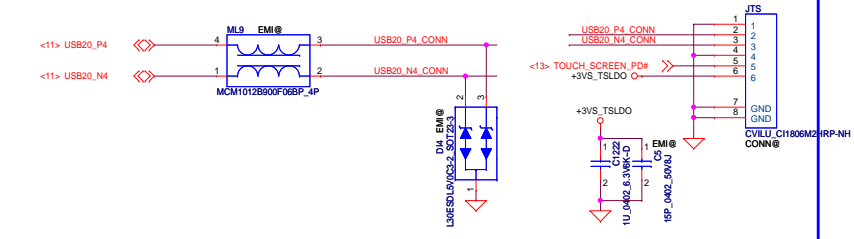
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					Size	Document Number	Rev
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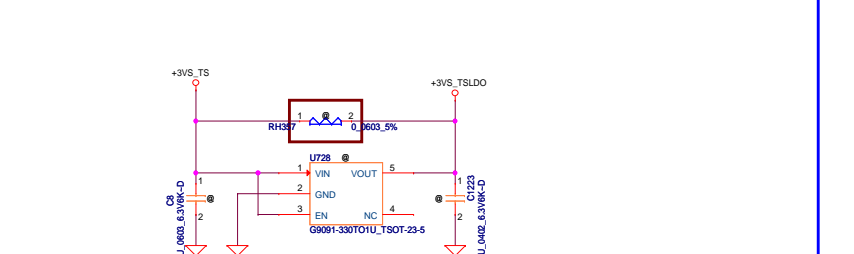
Camera



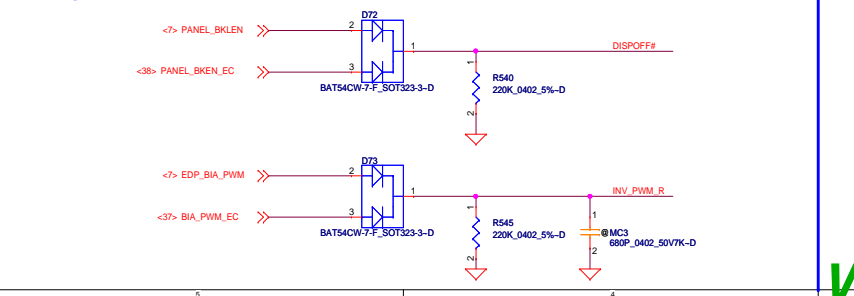
Touch Screen



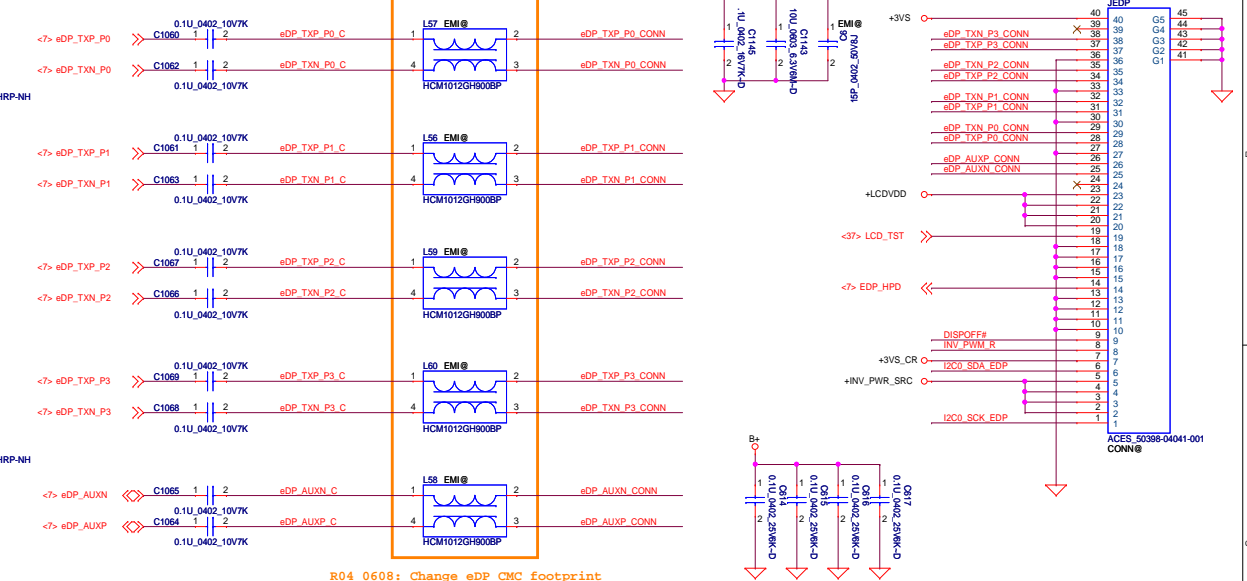
Touch Screen LDO



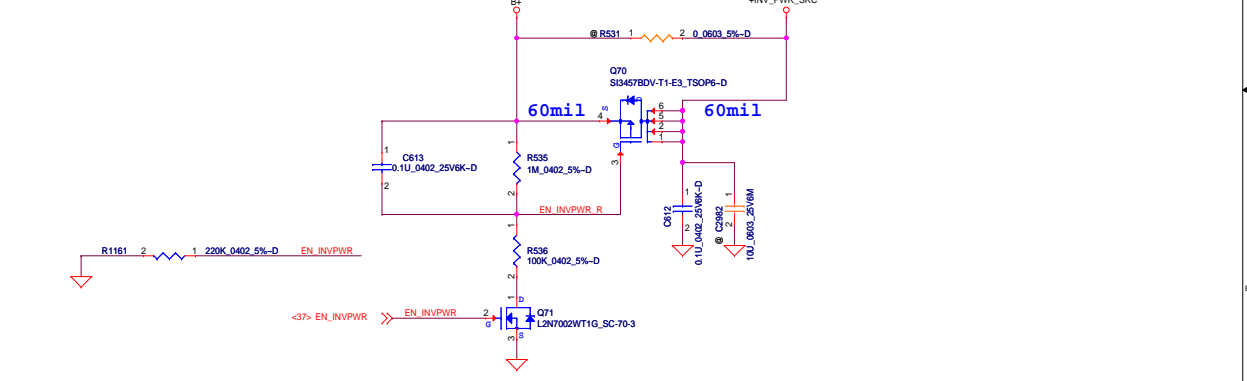
BackLight PWM Control



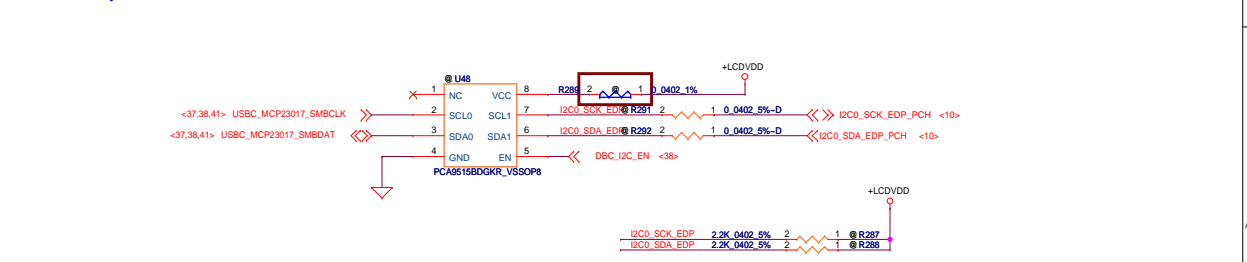
eDP Conn



eDP BackLight Power

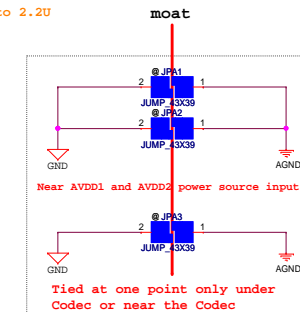
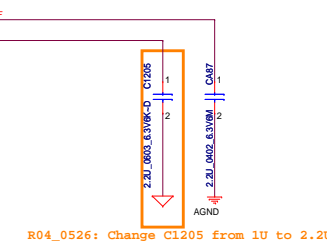
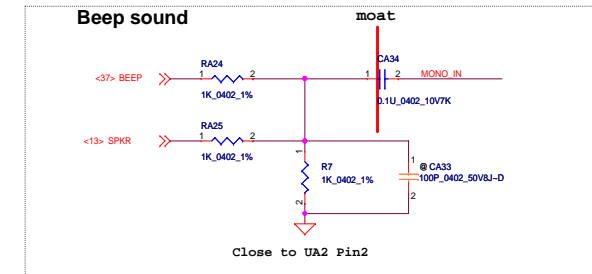
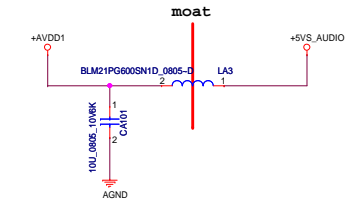
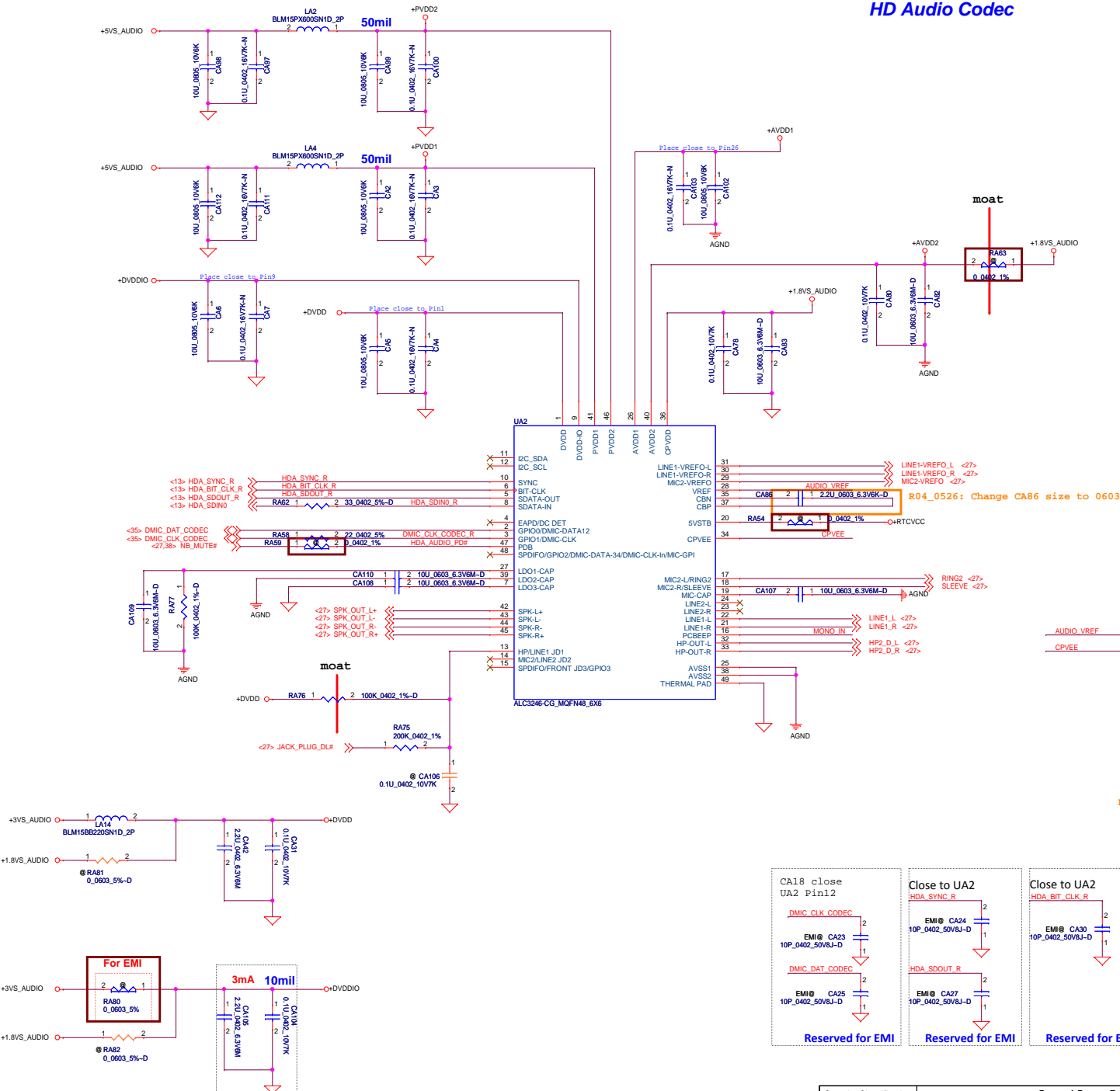


DBC delay schematic

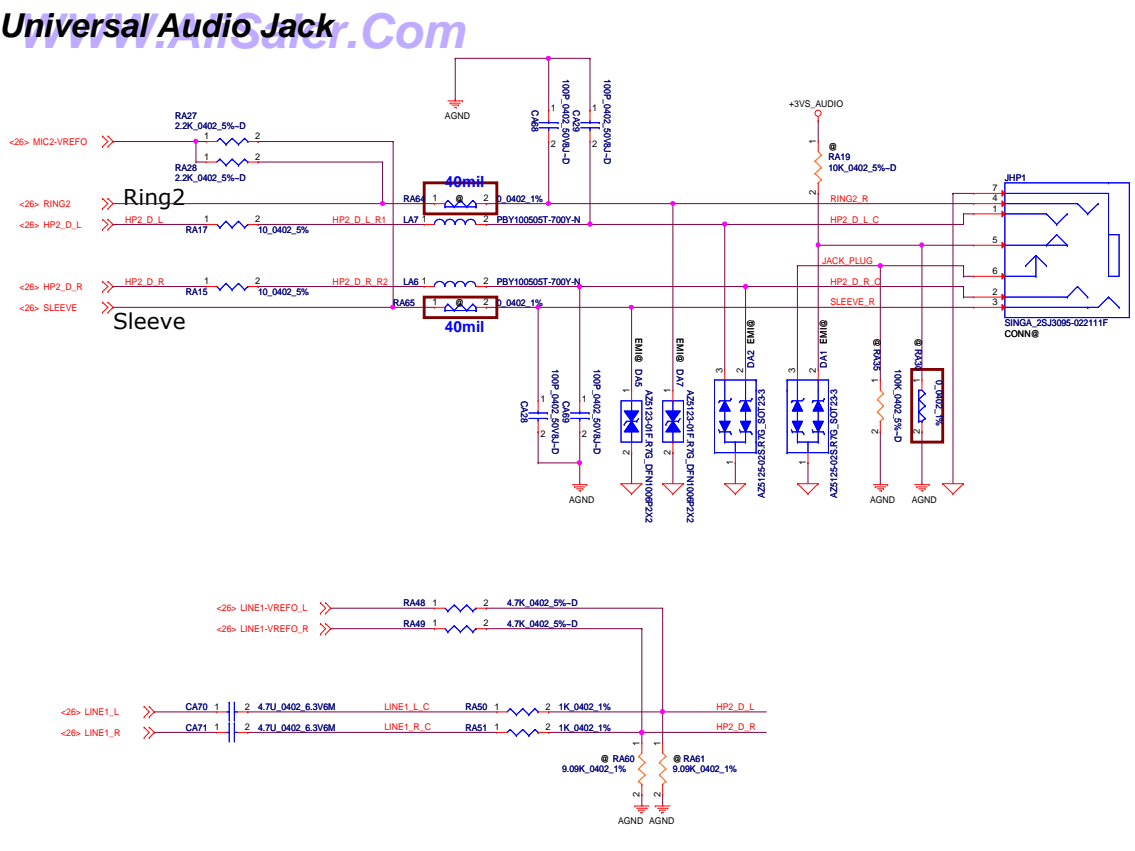


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Title			
P25-eDP/ Camera CONN			
Size		Document Number	
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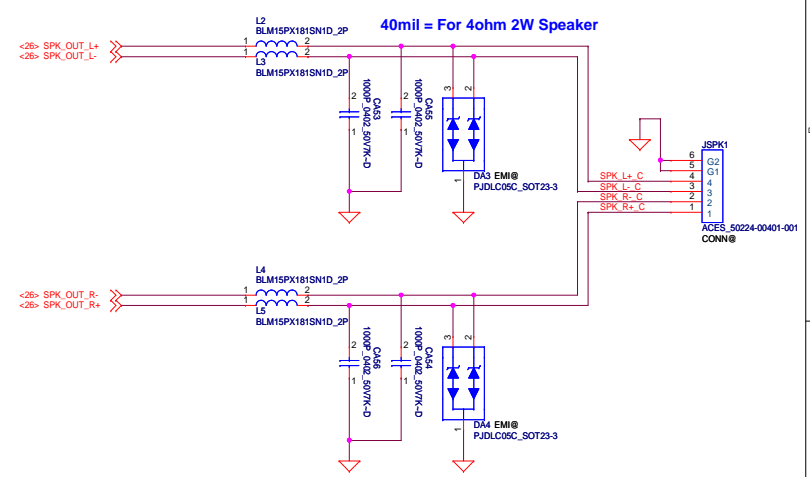
HD Audio Codec



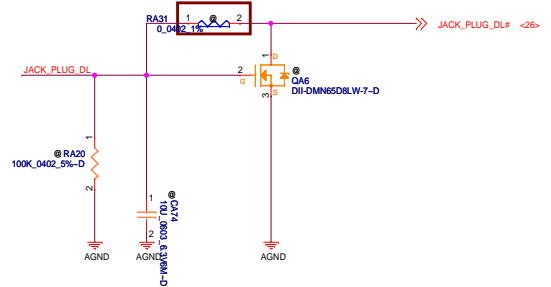
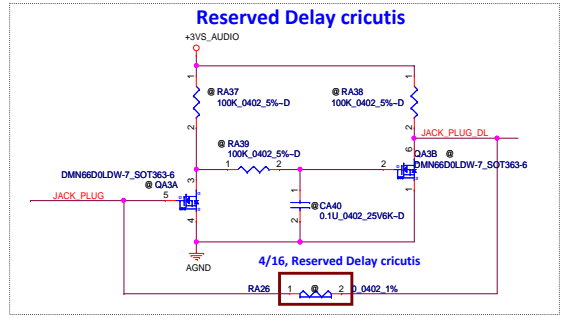
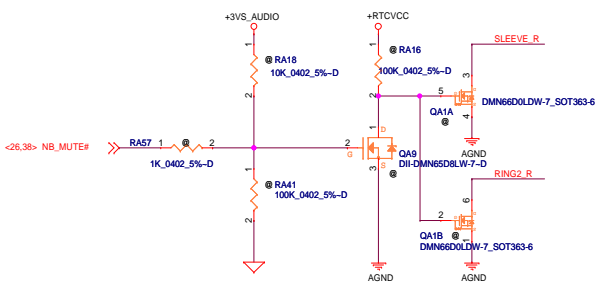
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Issued Date	2013/07/04	Deciphered Date	2013/10/28	Compal Electronics, Inc. P26-Audio Codec	
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Int. Speaker Conn.

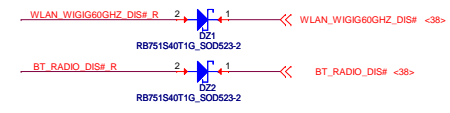
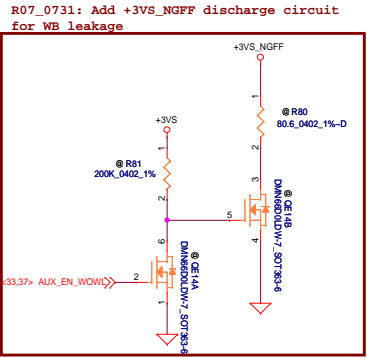
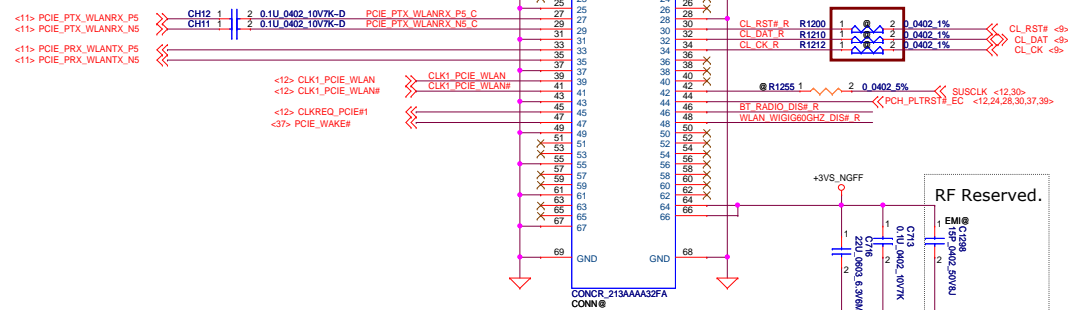
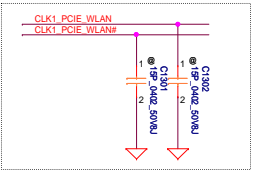
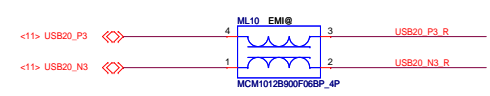


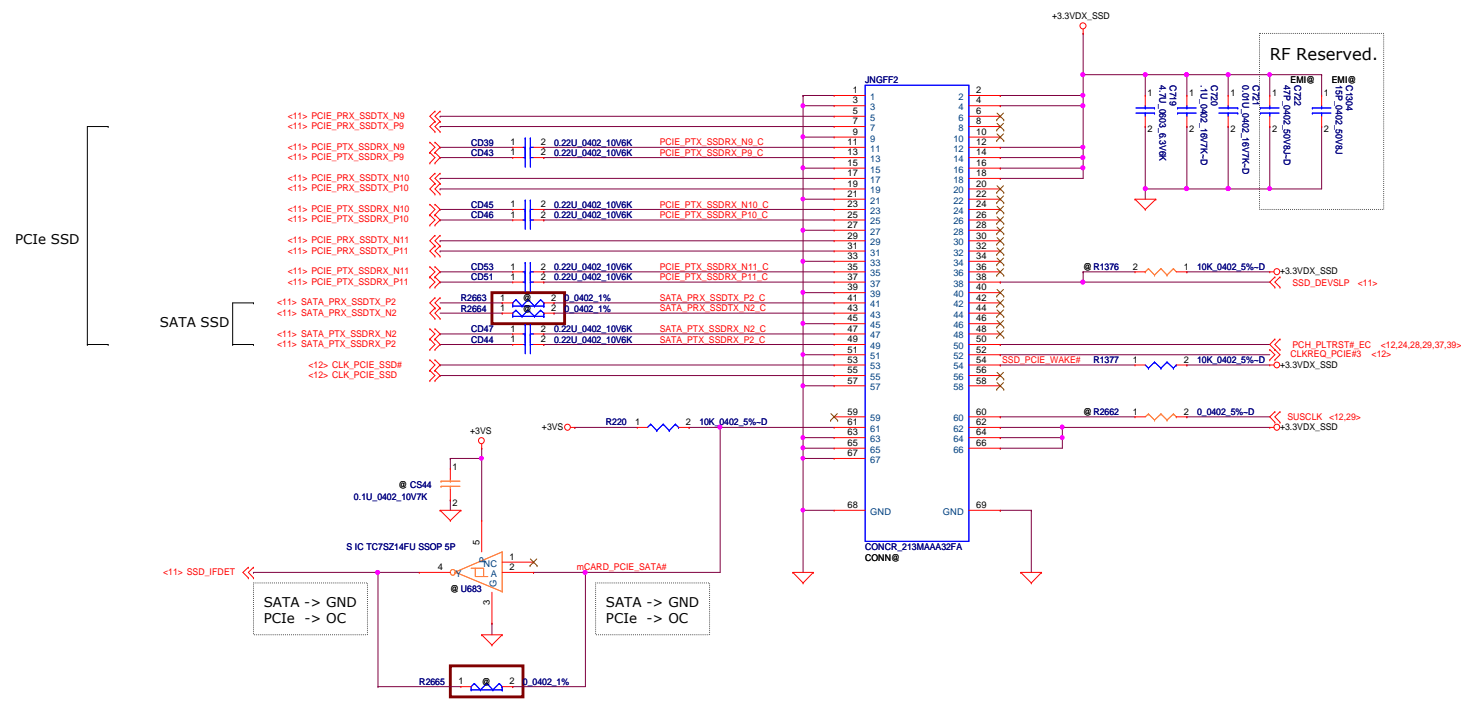
Prevent S3/S4/S5 Background Noise.
ALC3234/3246 has already integrated this grounding circuit inside the pin20



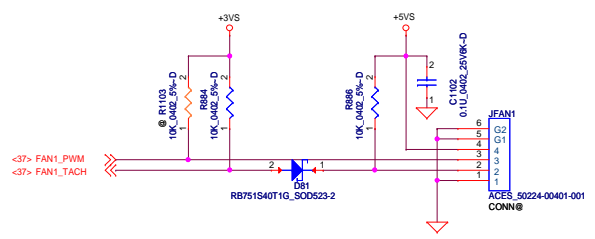
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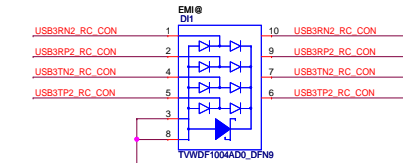
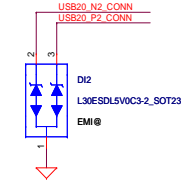
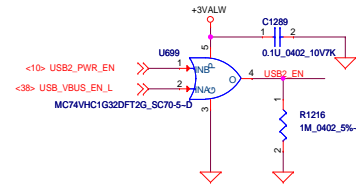
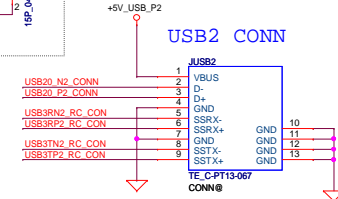
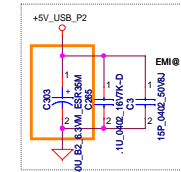
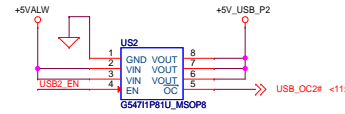
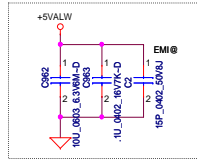
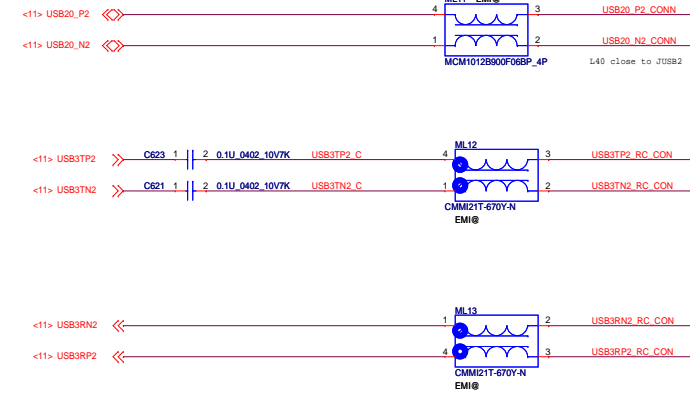
Security Classification	Compal Secret Data	Document Number	P27-Audio Jack / Speaker
Issued Date	2013/07/04	Deciphered Date	2013/10/28
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Date		Tuesday, October 13, 2015	Sheet 27 of 59





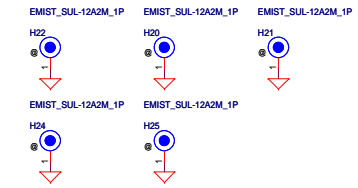
FAN





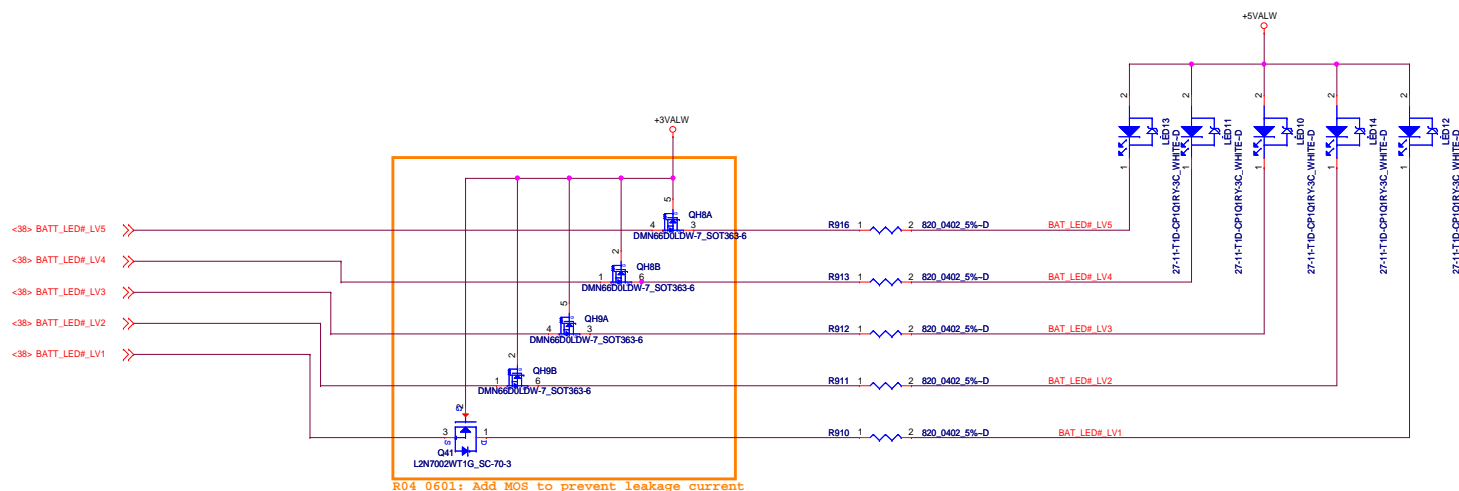
Hank0225: Note, PCB footprint is different from TVWDF1004AD0_DFN9, but it's compatible.

USB3.0 Shielding Clip



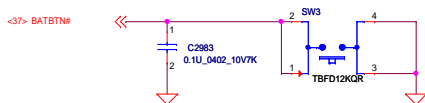
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Issued Date				Deciphered Date				Compal Electronics, Inc.			
2013/07/04				2013/10/28				P31-USB 3.0 IO CONN			
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Battery Gauge LED



R04_0601: Add MOS to prevent leakage current

Battery Gauge Button

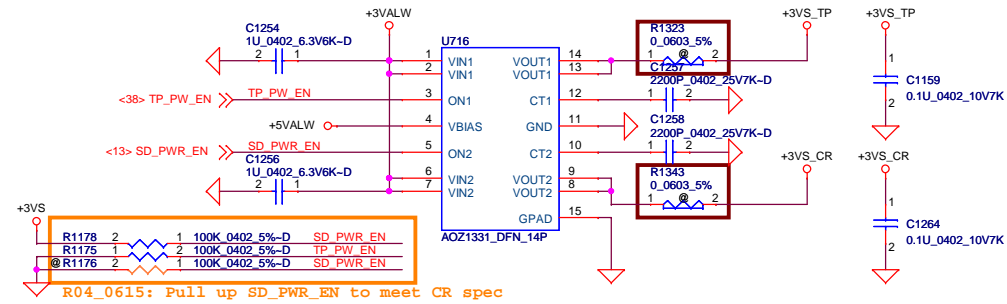


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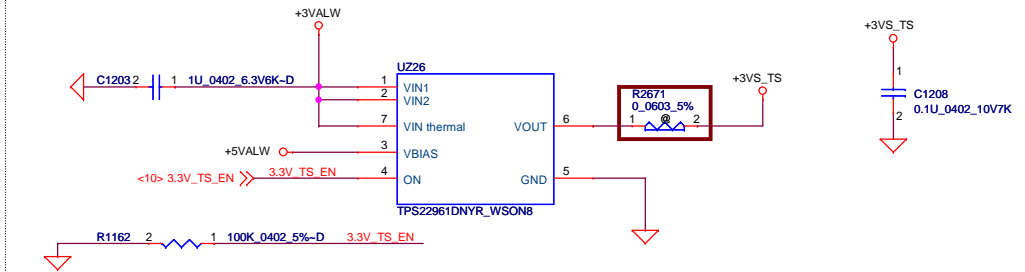
Compal Electronics, Inc.

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Issued Date	2013/07/04	Deciphered Date	2013/10/28	P32-BAT LED
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				Document Number
				LA-C881P
				Rev
				1.0
				Date
				Tuesday, October 13, 2015
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				32 of 59

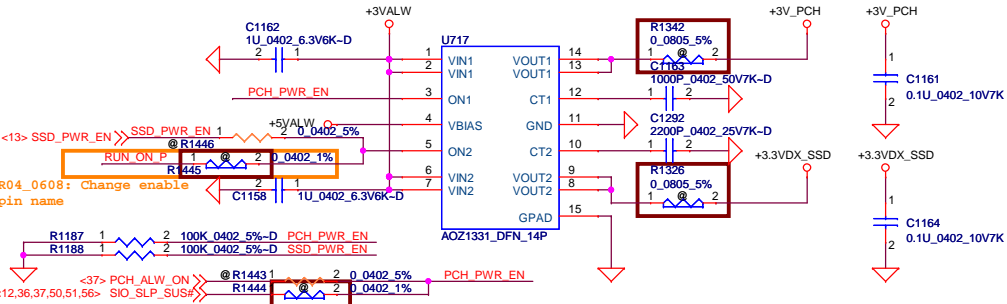
Touch Pad, Card Reader Load Switch



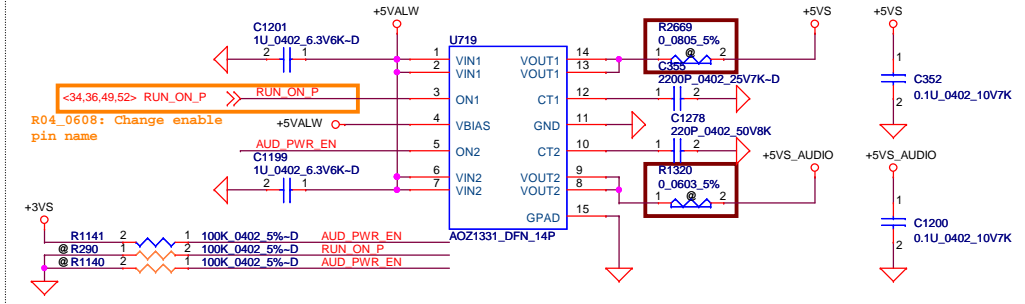
Touch Screen Load Switch



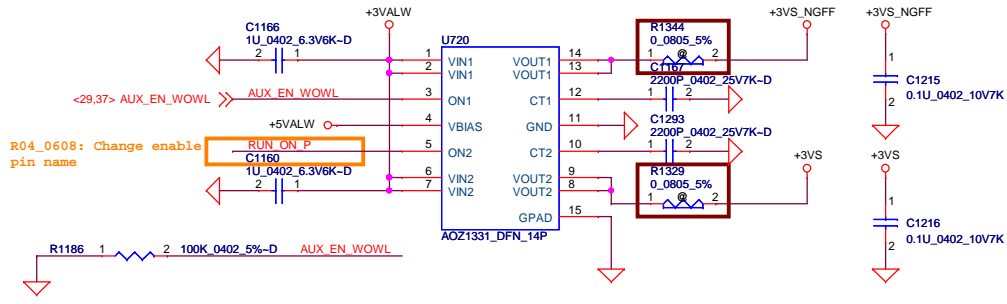
Deeper Sleep, SSD Load Switch



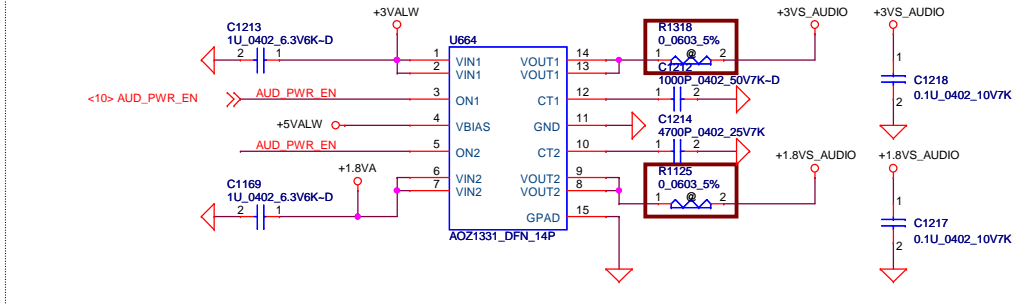
5V_Run, 5V_Audio Load Switch



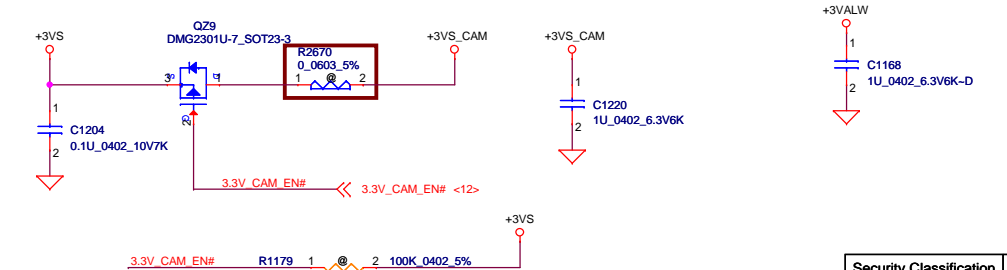
WiFi, 3V_RUN Load Switch



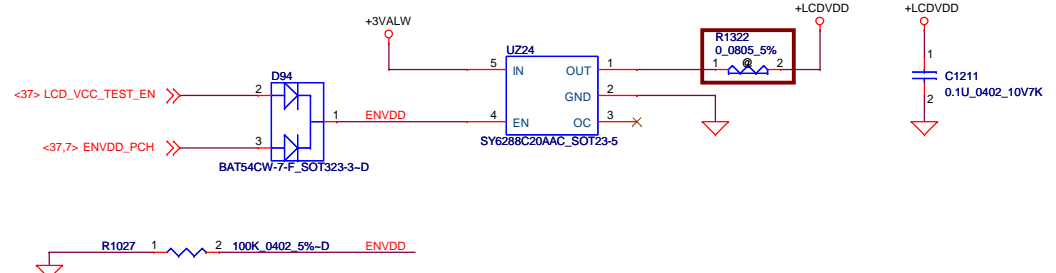
3V_Audio, 1.8V_Audio Load Switch



Camera

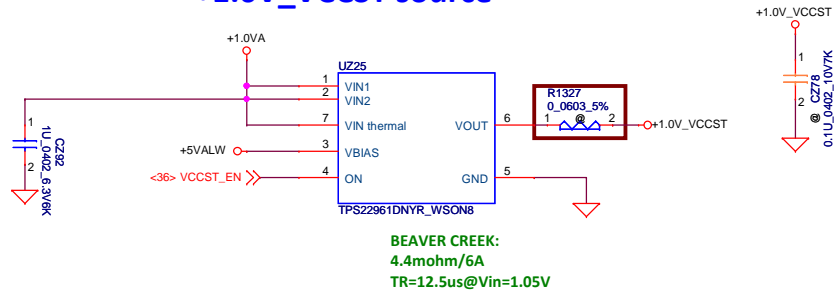


LCD Load Switch

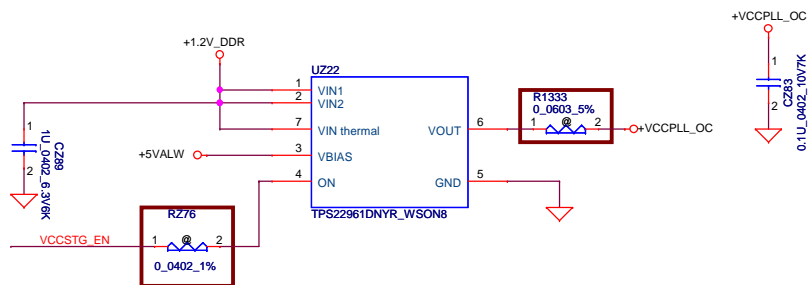


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Date				Tuesday, October 13, 2015				Document Number			
Sheet				33				Rev			
of				59				LA-C881P			
1.0											

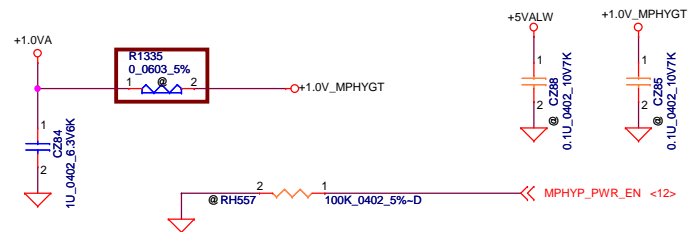
+1.0V_VCCST source



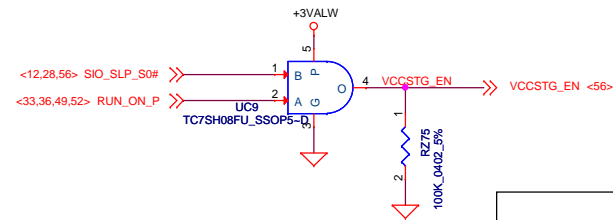
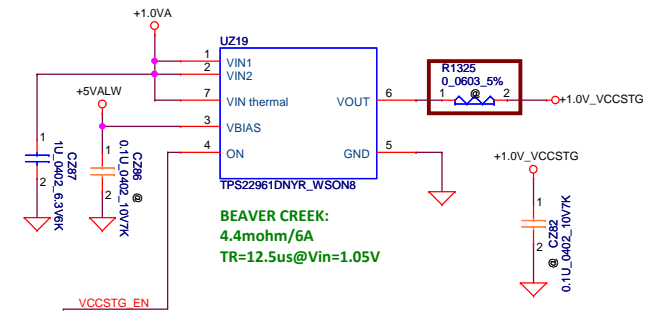
+VCCPLL_OC source



+1.0V_MPHYGT source

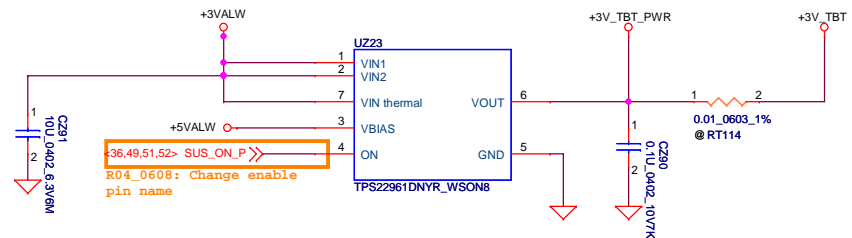


+1.0V_VCCSTG source



	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

TBT Power circuits

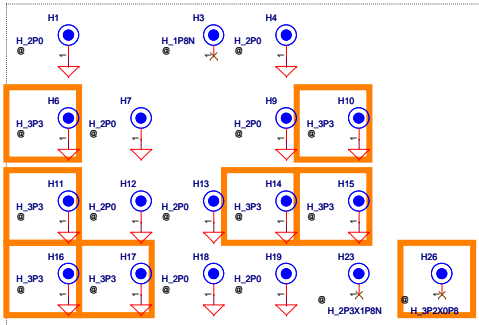
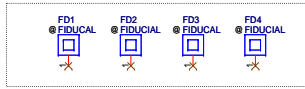


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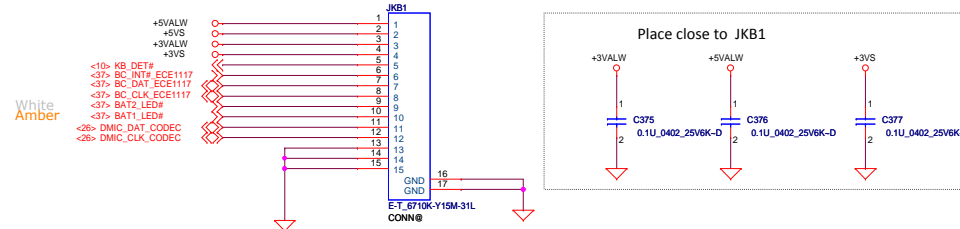
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Title		P34-DC/DC Interface 2	
Size	Document Number	Rev	
	LA-C881P	1.0	
Date:	Tuesday, October 13, 2015	Sheet	34 of 59



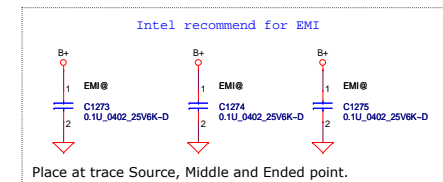
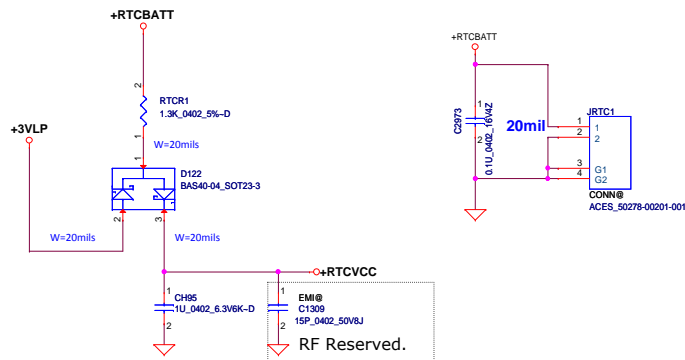
R06_0822: Stand off screw hole change form 3.2mm to 3.3 mm.
R06_0826: Add H26 for SSD bracket.

Keyboard Controller board + DMIC

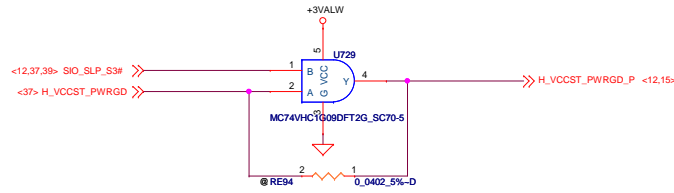


RTC Battery With Charge Function

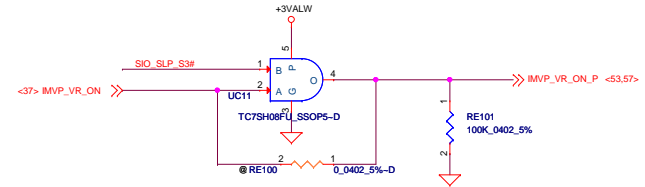
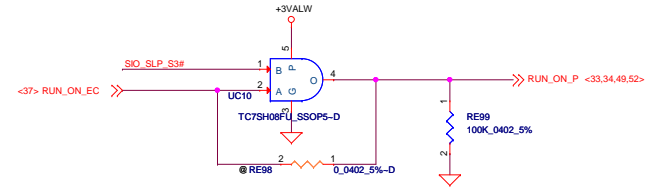
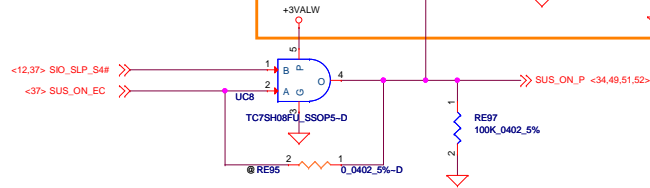
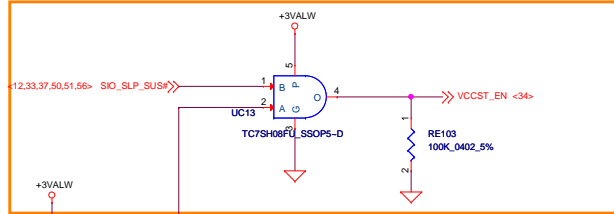
RTC Battery Conn



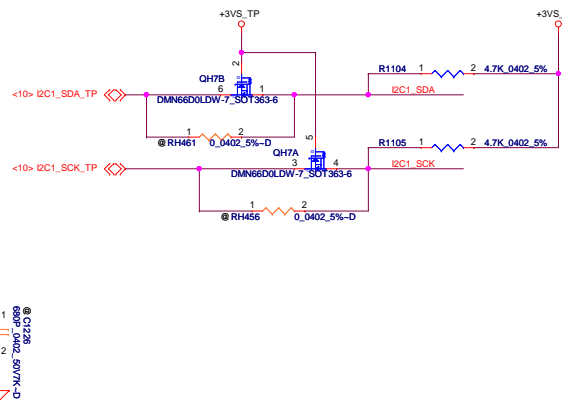
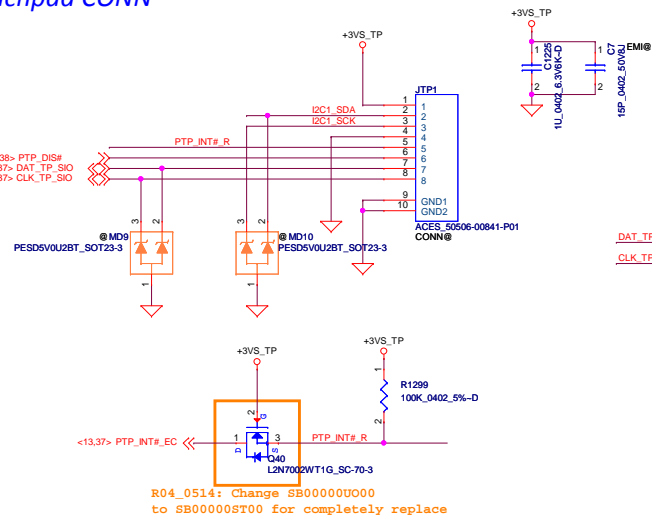
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				Size	Document Number
				LA-C881P	Rev 1.0
				Date:	Tuesday, October 13, 2015
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R04_0604: Add VCCST enable condition for deep S3 power state & sequence

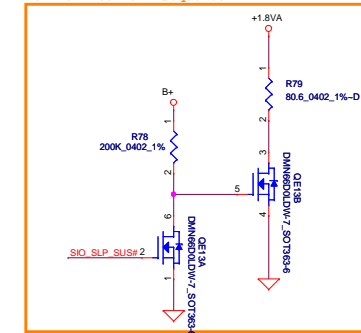


Touchpad CONN

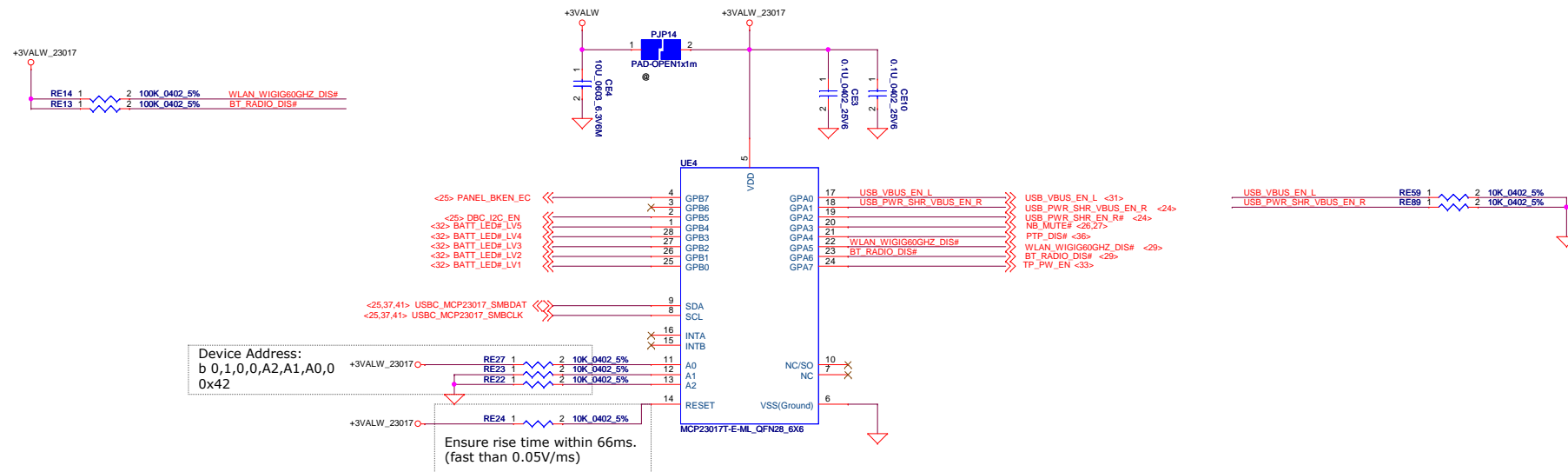


+1.8VA Discharge

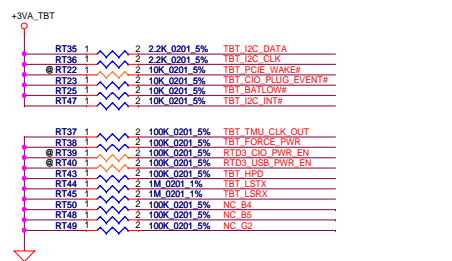
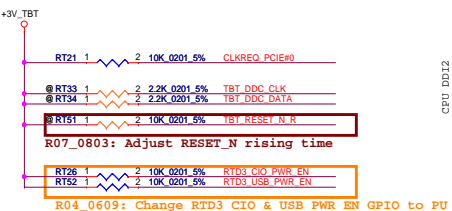
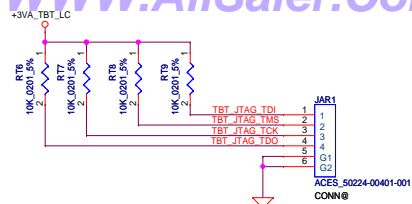
R04_0612: Add +1.8VA discharge circuit for rail to rail sequence



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				P36-TP/PWGRGD/LID	
				Document Number	
				LA-C881P	
				Rev	
				1.0	
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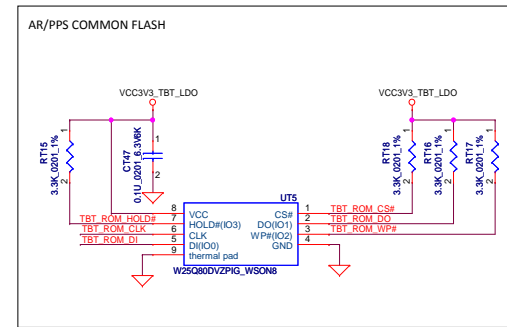
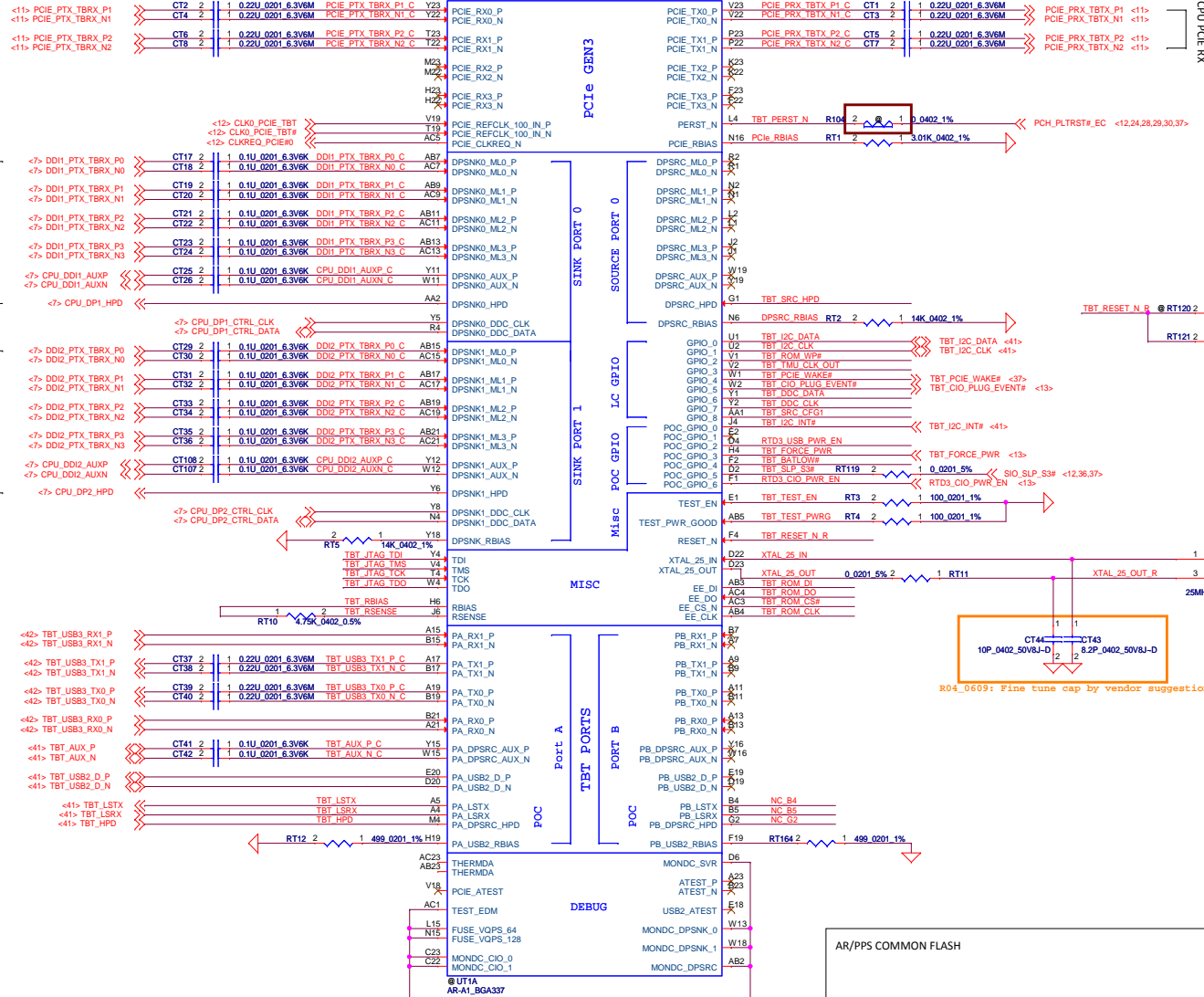


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				Document Number		LA-C381P	
				Date		Tuesday, October 13, 2015	
				Sheet		38 of 59	
				Rev		1.0	

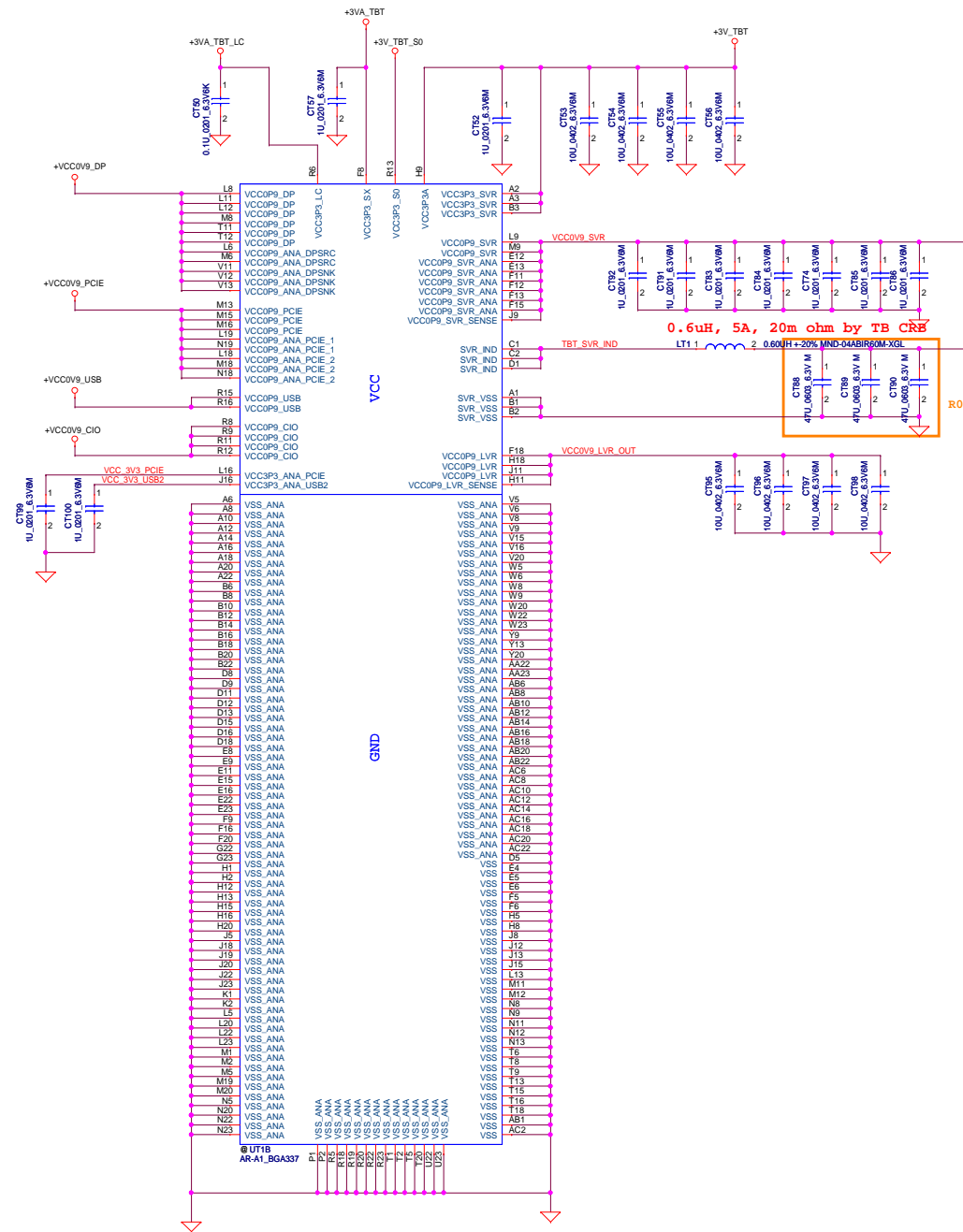
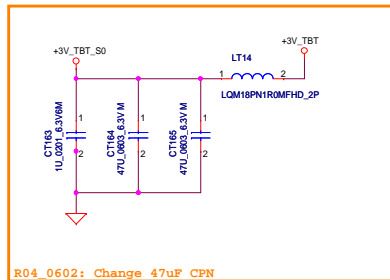
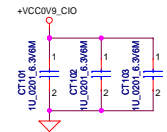
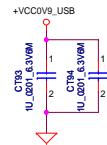
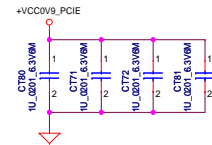
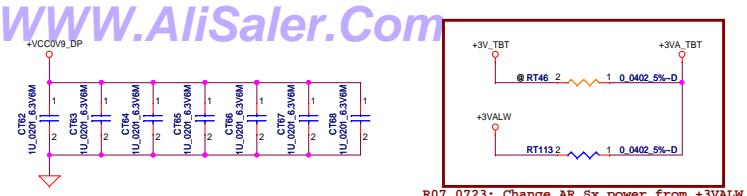


NOTE:
ASSEMBLE R297, R299 if DPSRC
NOT IN USE

TBT_SRC_CFG1 R1403 1 2 1M 0.001 1%
TBT_SRC_HPD R1405 1 2 1M 0.001 1%



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Size	C	Sheet	39 of 59
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R04_0602: Change 47uF CPN

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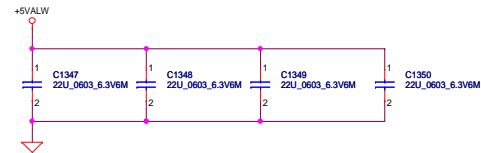
Compal Electronics, Inc.

P40-AR TBT (2/2) PWR / VSS

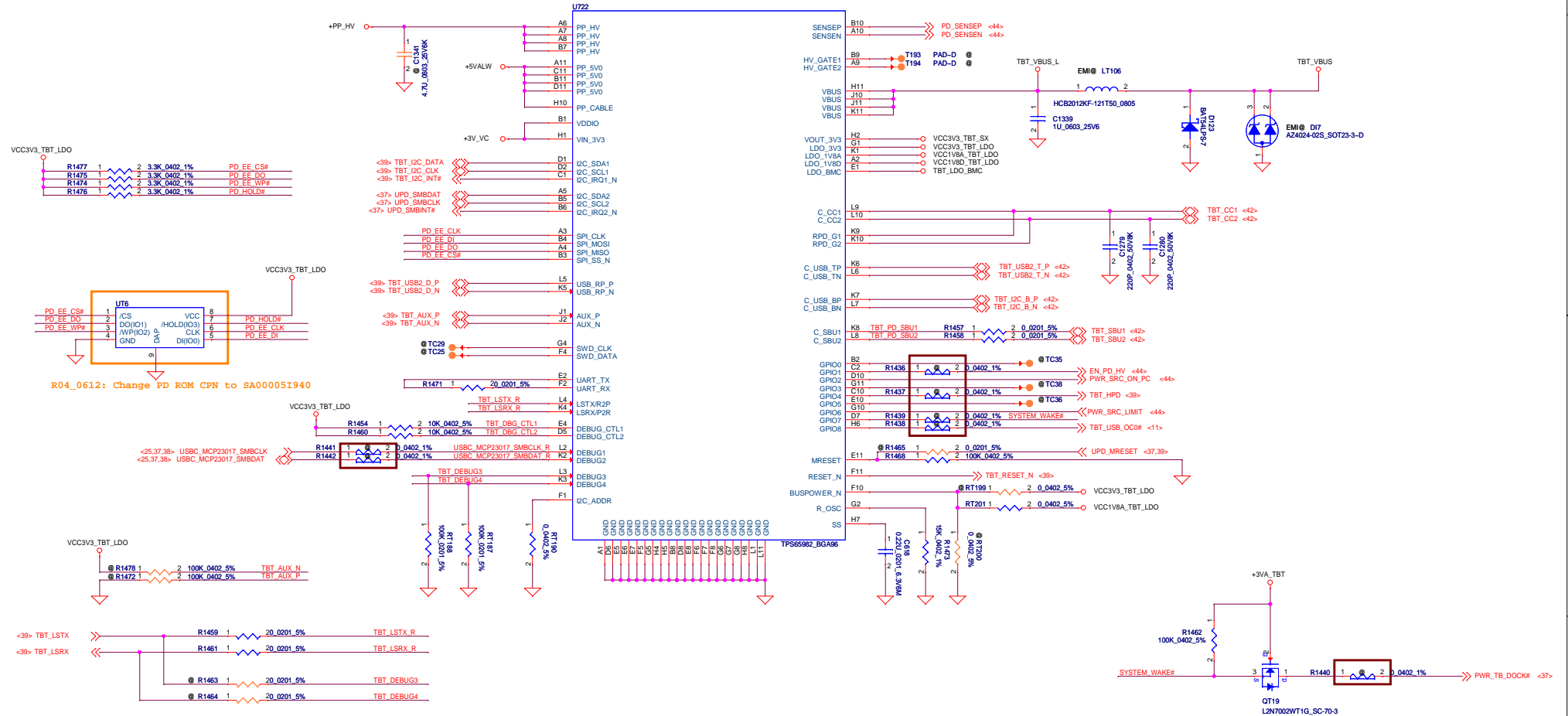
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Issued Date	2013/07/04	Deciphered Date
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Title	P40-AR TBT (2/2) PWR / VSS	
Size	Document Number	Rev
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Date:	Tuesday, October 13, 2015	Sheet 40 of 59


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R07_0720: Change "VCC5V0_SYS"
to "+5VALW"
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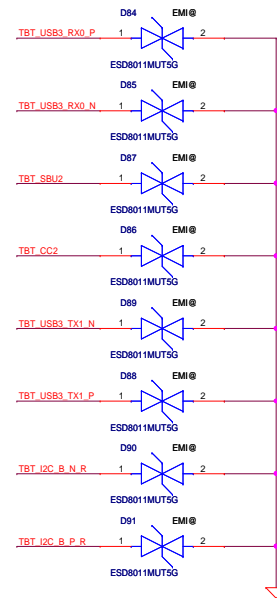
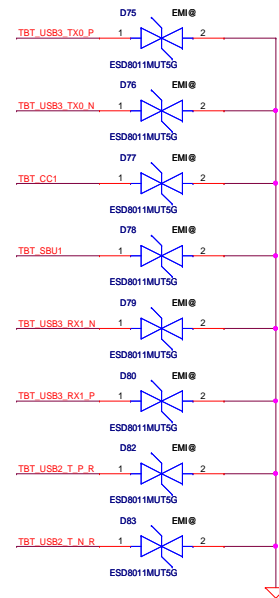
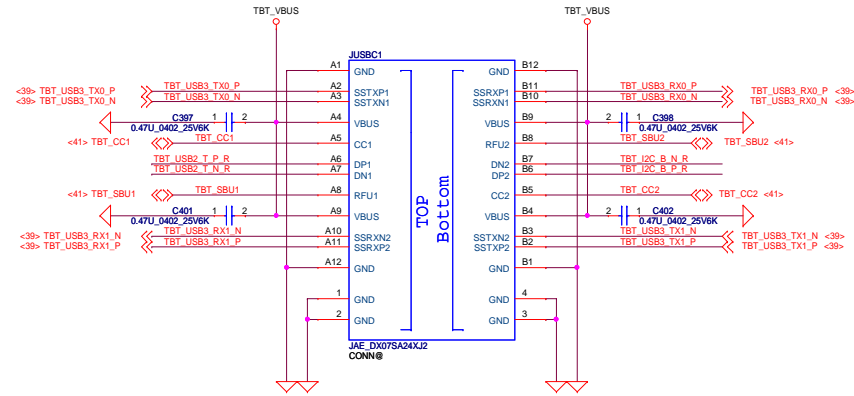
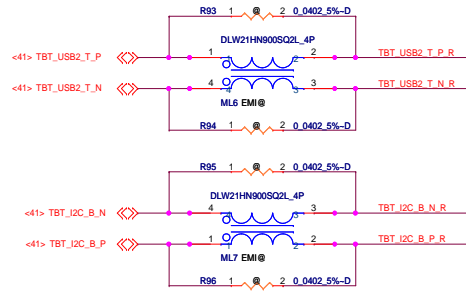


R07_0720: Change PD to MP CPN

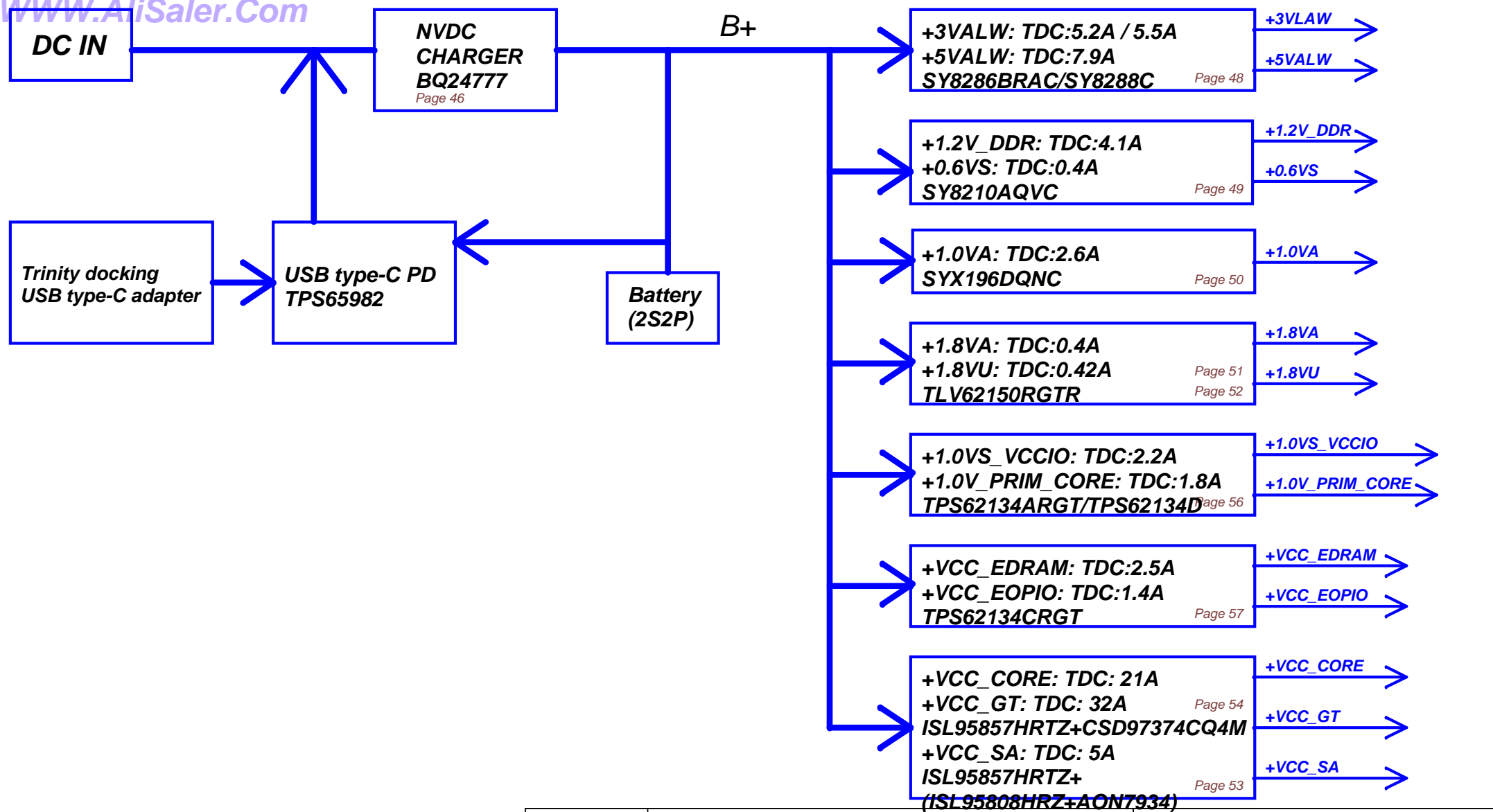


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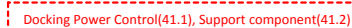
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Issued Date	2013/07/04	Deciphered Date	2012/07/25	Title	P41-PD CONTROL LA-C881P
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LA-C881P		Rev		1.0	
Date: Tuesday, October 13, 2015		Sheet		42 of 59	



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				Size
				Document Number
				LA-C881P
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				Date: Tuesday, October 13, 2015
				Sheet 43 of 59

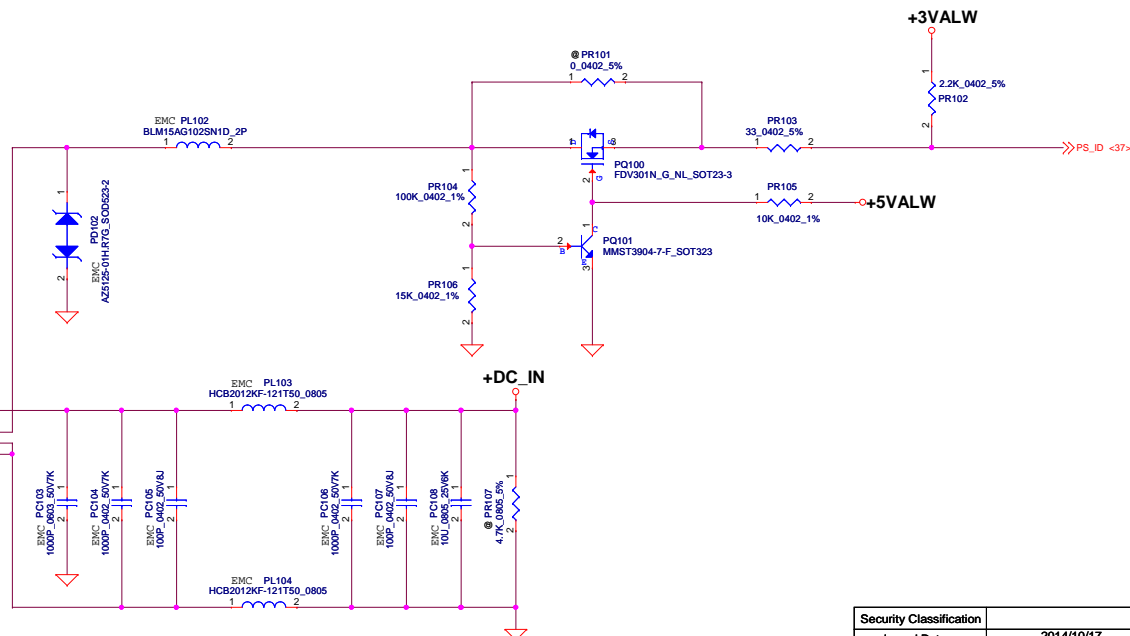
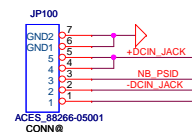
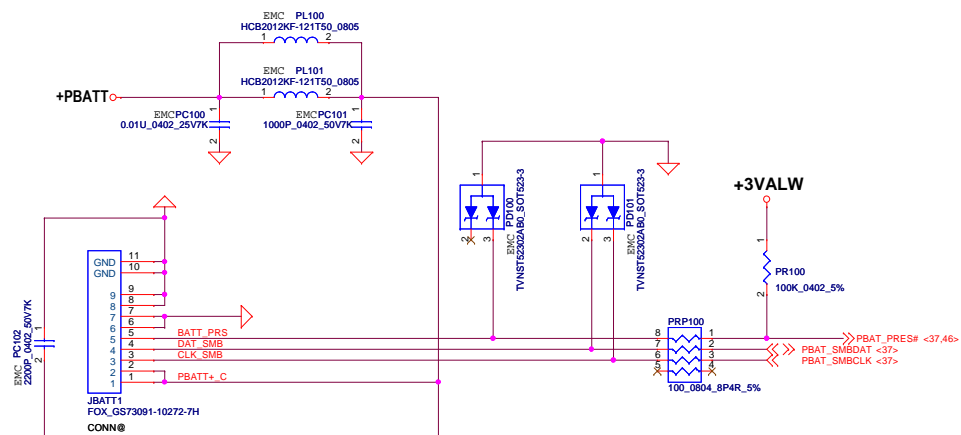


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Issued Date	2014/10/17	Deciphered Date	2014/12/05	P44-PWR Switch	
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PBATT1 connector

SMART Battery:

- 1.BATT++
- 2.BATT++
- 3.CLK_SMB
- 4.DAT_SMB
- 5.BAT_PRS
- 6.SYS_PRES
- 7.BAT_ALERT
- 8.GND
- 9.GND
- 10.GND
- 11.GND



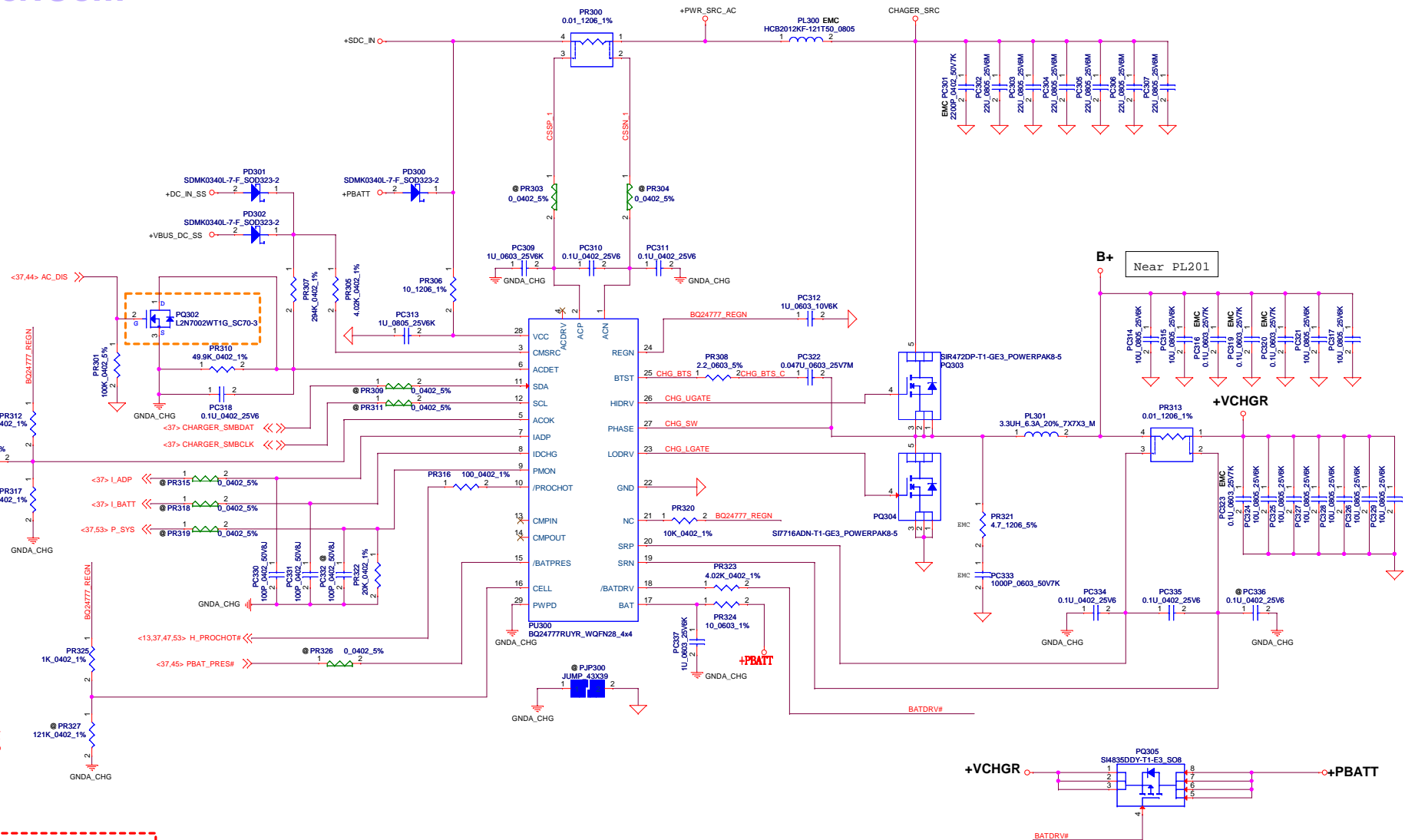
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	PWR45 DCIN/BATT CONN
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PQ302
main:SB000000ST00
2nd:SB000000U000
3rd:SB000000Z600

CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side

TI FAE_Andrew suggest
Cell pin set the voltage of
three cell (13.5V) for OVP

Charger controller(40.1), Support component(40.2)

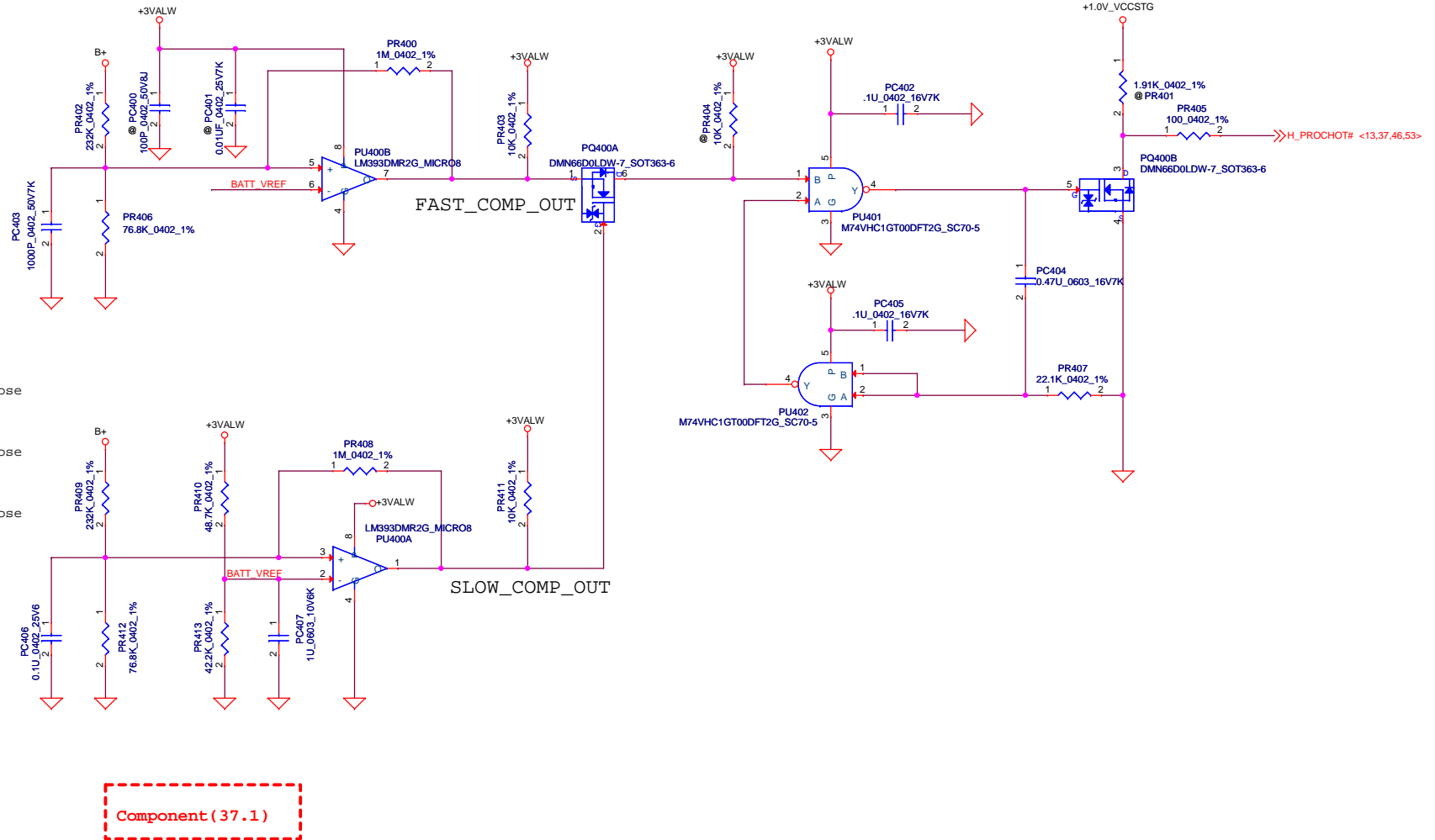


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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	P46-PWR Charger
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PU404_Main source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.05V PA409A close

PU404_2nd_source
PQ409A open at 3/5V_B+ below 5.72V
and 3/5V_B+ recover 6.05V PA409A close

PU404_3rd_source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.04V PA409A close



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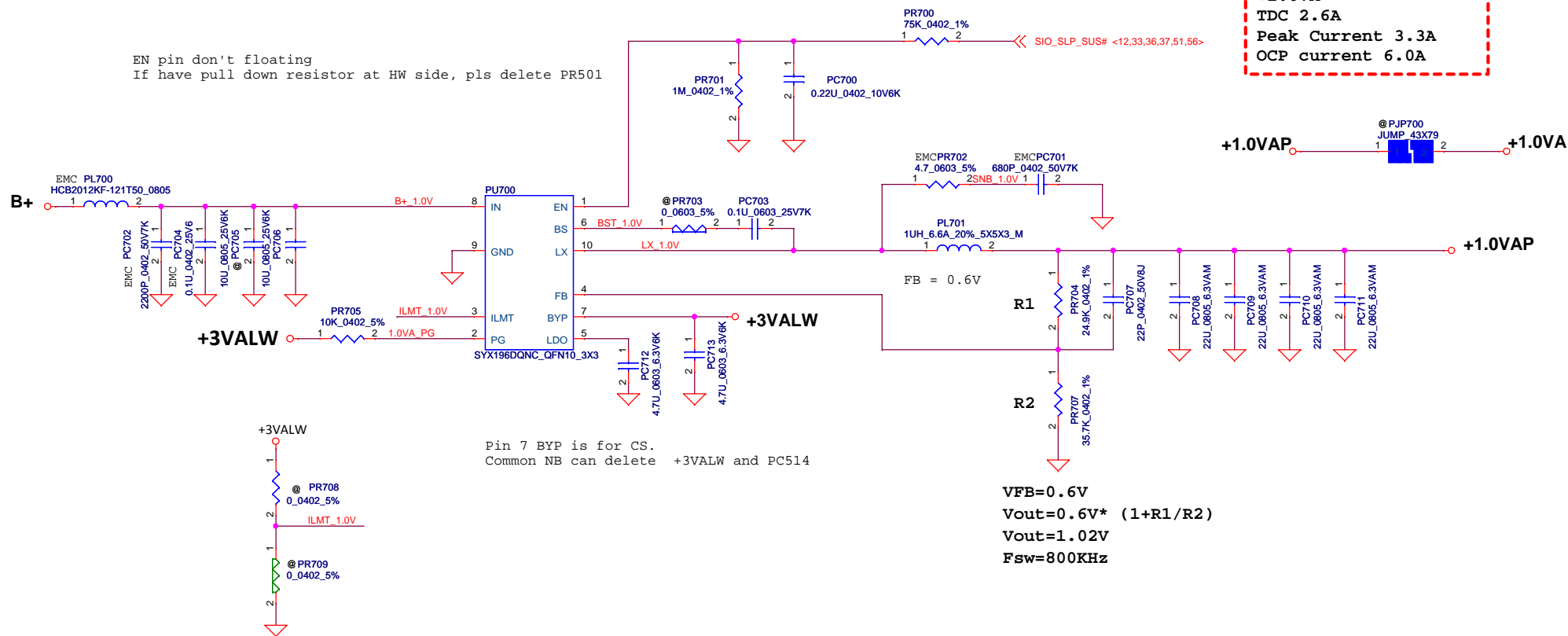
+1.2V_DDR TDC 4.1A Peak Current 5.8A OCP Current 8A	0.6Volt +/- 5% TDC 0.4A Peak Current 0.6A OCP Current 2A (fix)
--	---

DDR controller(35.3), Support component(35.4)

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

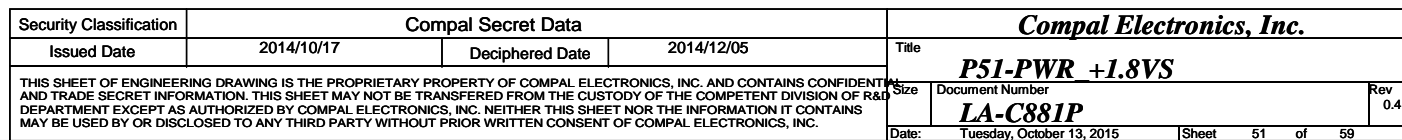
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title P49-PWR +1.2V DDR/0.6VS		
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					LA-C881P	0.4
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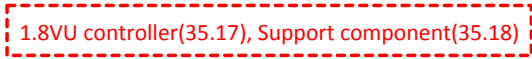


The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high.
OCP setting 6A

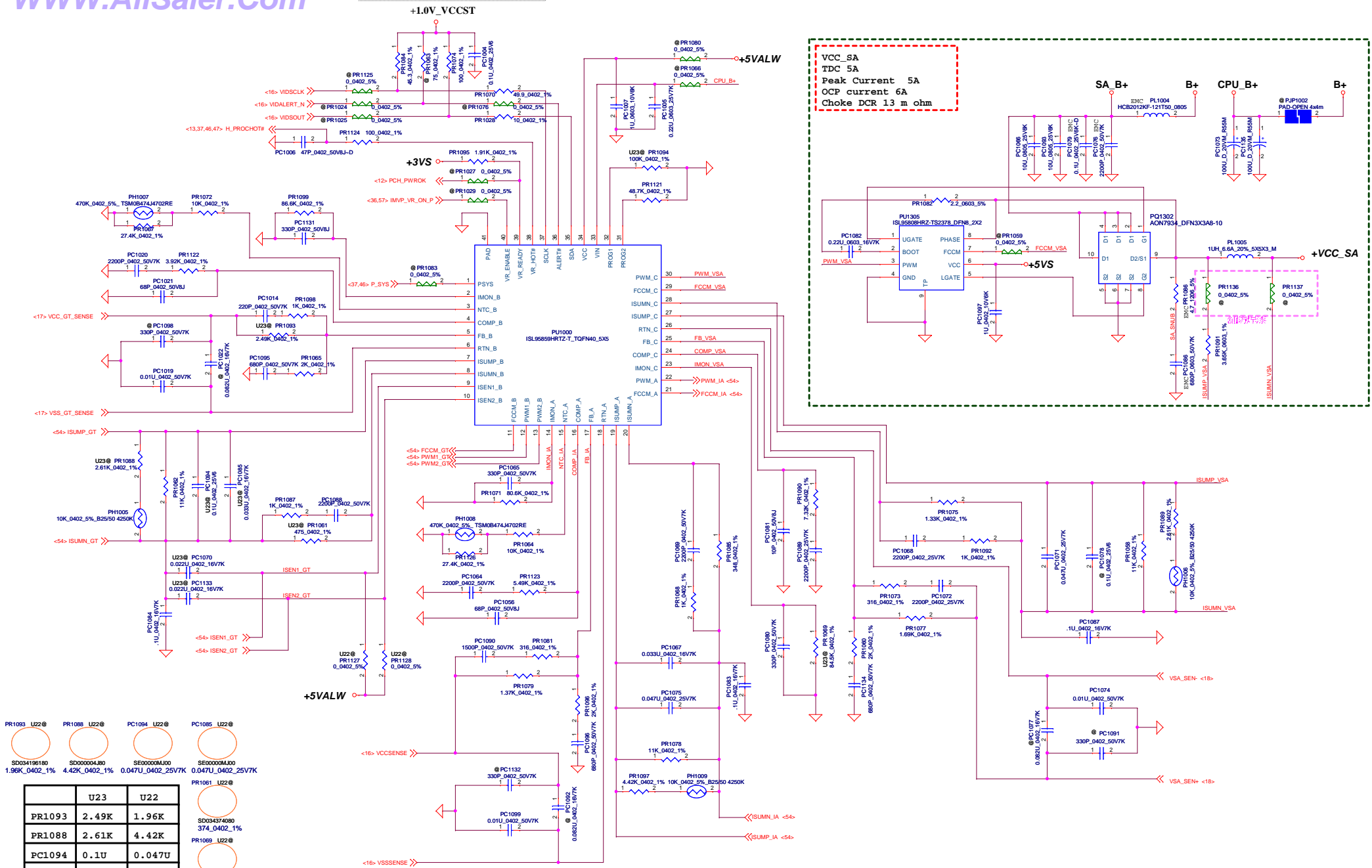
1.05V controller(35.5), Support component(35.6)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	P50-PWR +1.0VA
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				Size	Document Number
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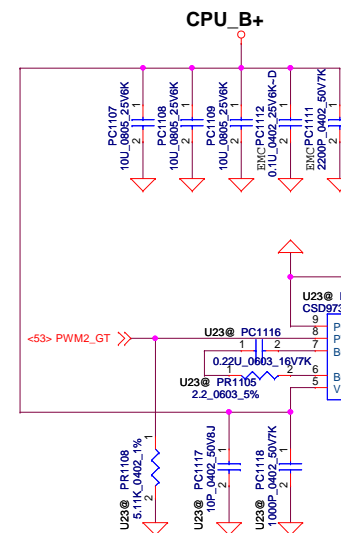
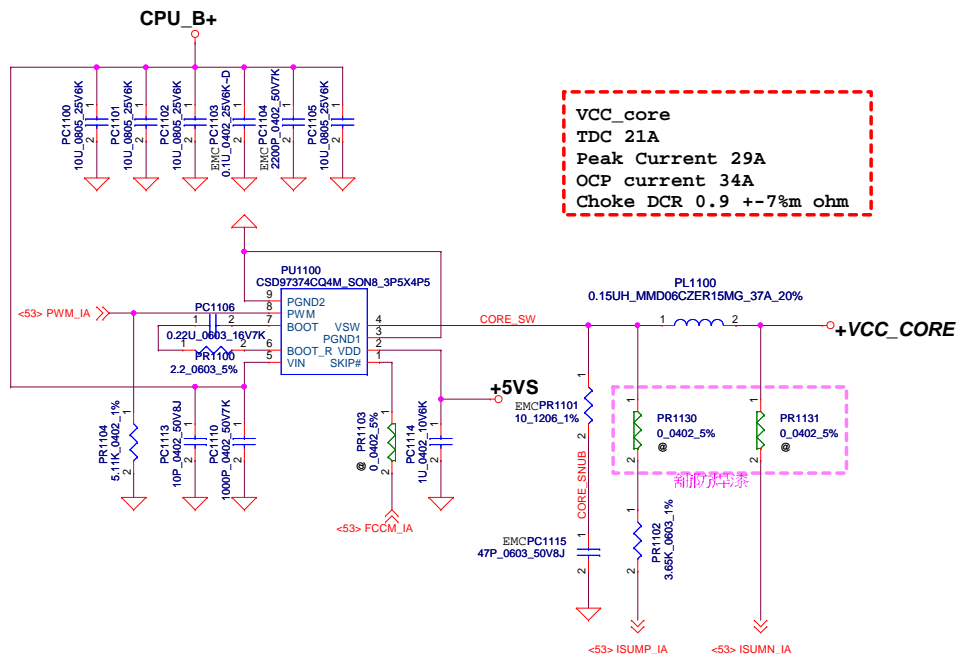
PR1093 U22@	PR1088 U22@	PC1094 U22@	PC1095 U22@
SD034196180	SD00000480	SE00000M00	SE00000M00
1.96K_0.402_1%	4.42K_0.402_1%	0.047U_0.402_25V7K	0.047U_0.402_25V7K

	U23	U22
PR1093	2.49K	1.96K
PR1088	2.61K	4.42K
PC1094	0.1U	0.047U
PC1095	0.033U	0.047U
PR1061	475	374
PR1069	84.5K	124K
PR1094	100K	78.7K

PR1061 U22@	SD034374080
	374_0.402_1%
PR1069 U22@	SD034124380
	124K_0.402_1%
PR1094 U22@	SD034787280
	78.7K_0.402_1%

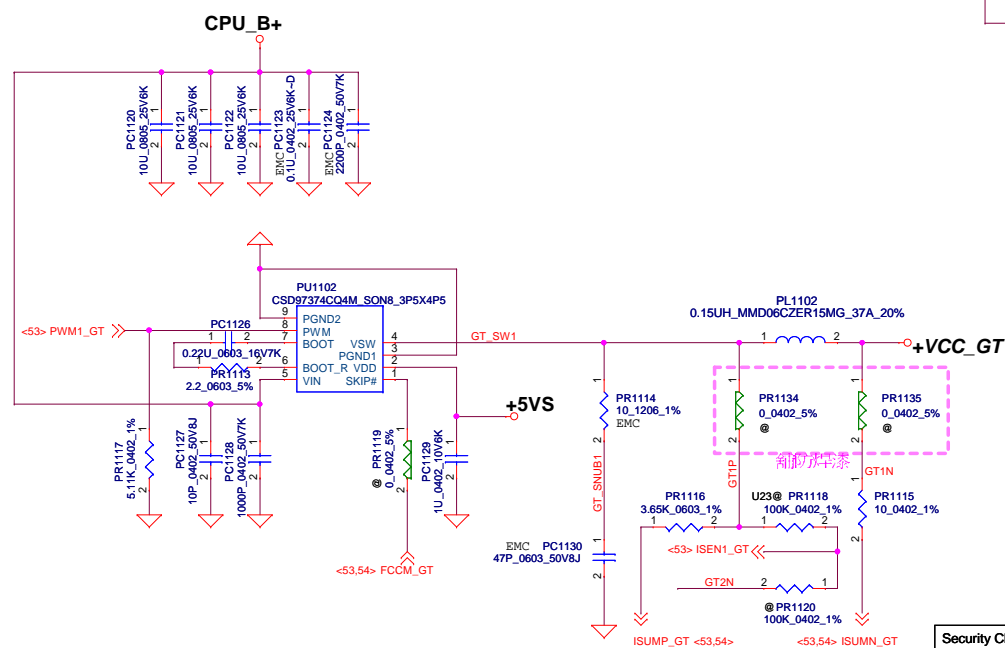
VCC_CORE controller(36.1), Drivers (36.2), Support component(36.3)

Security Classification		Compal Secret Data	
Issued Date	2014/10/17	Deciphered Date	2014/12/05
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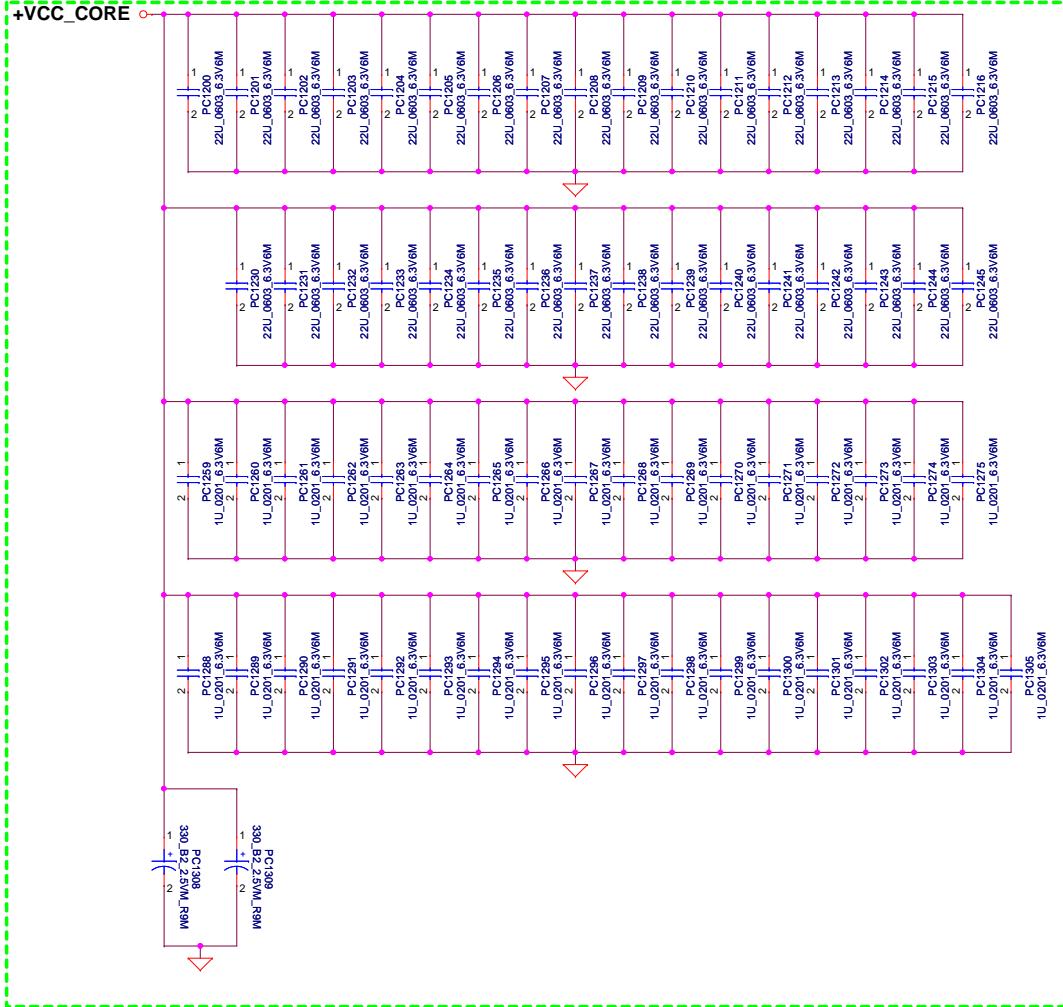


VCC_GT (U-line 23e)
TDC 32A
Peak Current 57A
OCP current 74A
Choke DCR 0.9 +-7% ohm

VCC_GTx
TDC 5A
Peak Current 7A



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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VCC_SA Place on CPU

TOP Side.

22U_0603 * 10 pcs + 1U_0201*7 pcs

Bottom Side.

22U_0603 * 2 pcs

VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

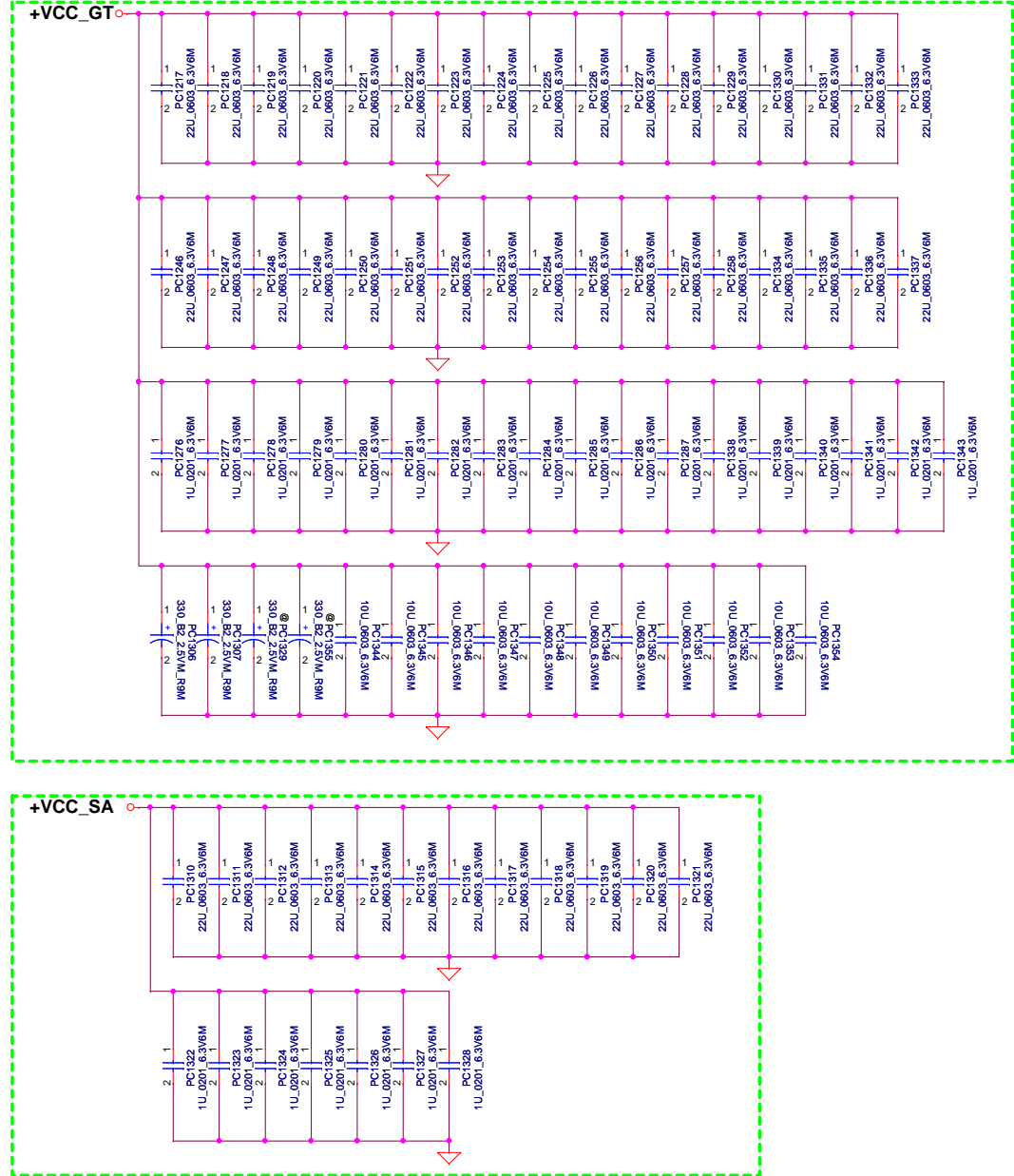
VCC_GT Place on CPU

TOP Side.

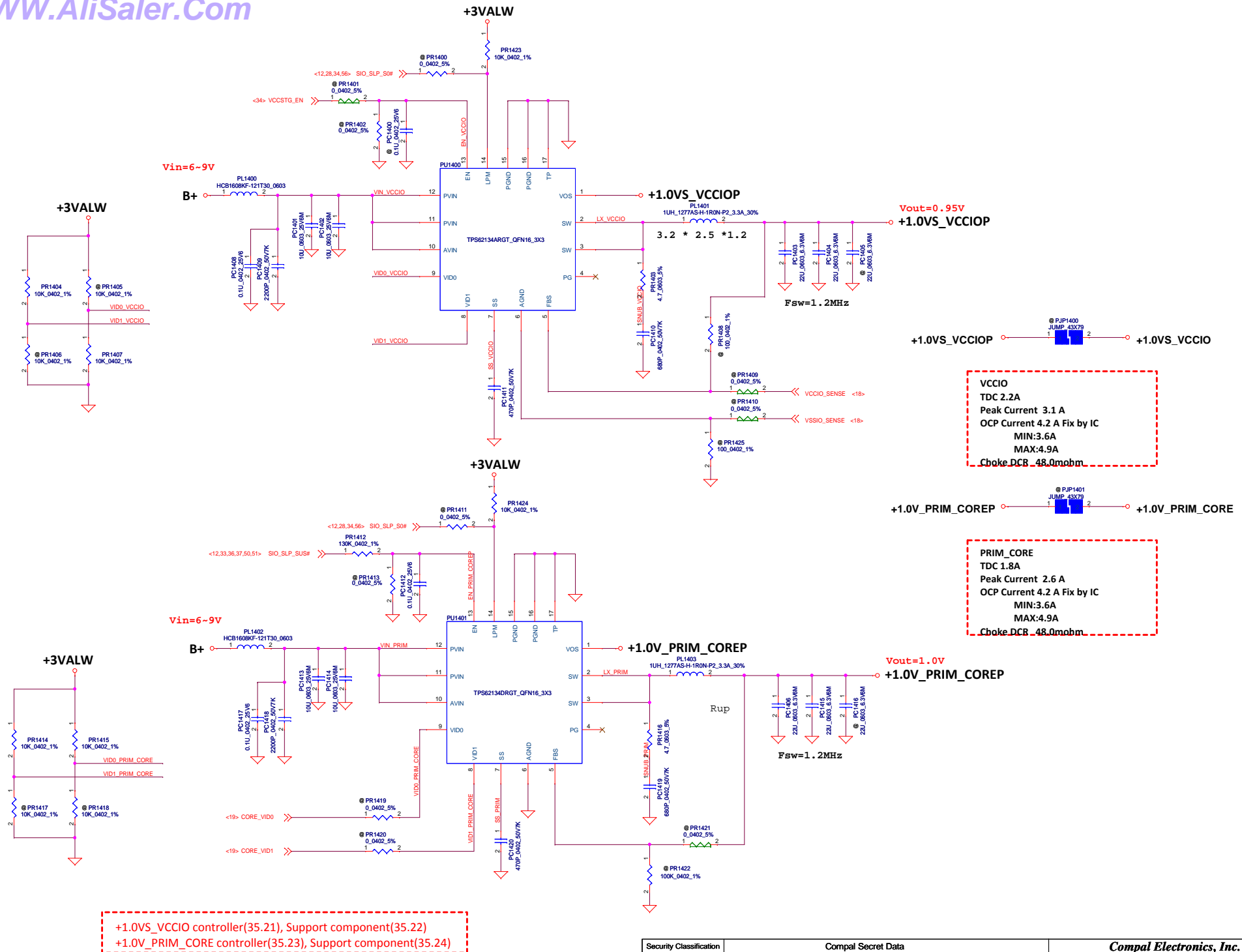
22U_0603 * 34 pcs +10U_0603*11 pcs +1U_0201*18 pcs

Bottom Side.

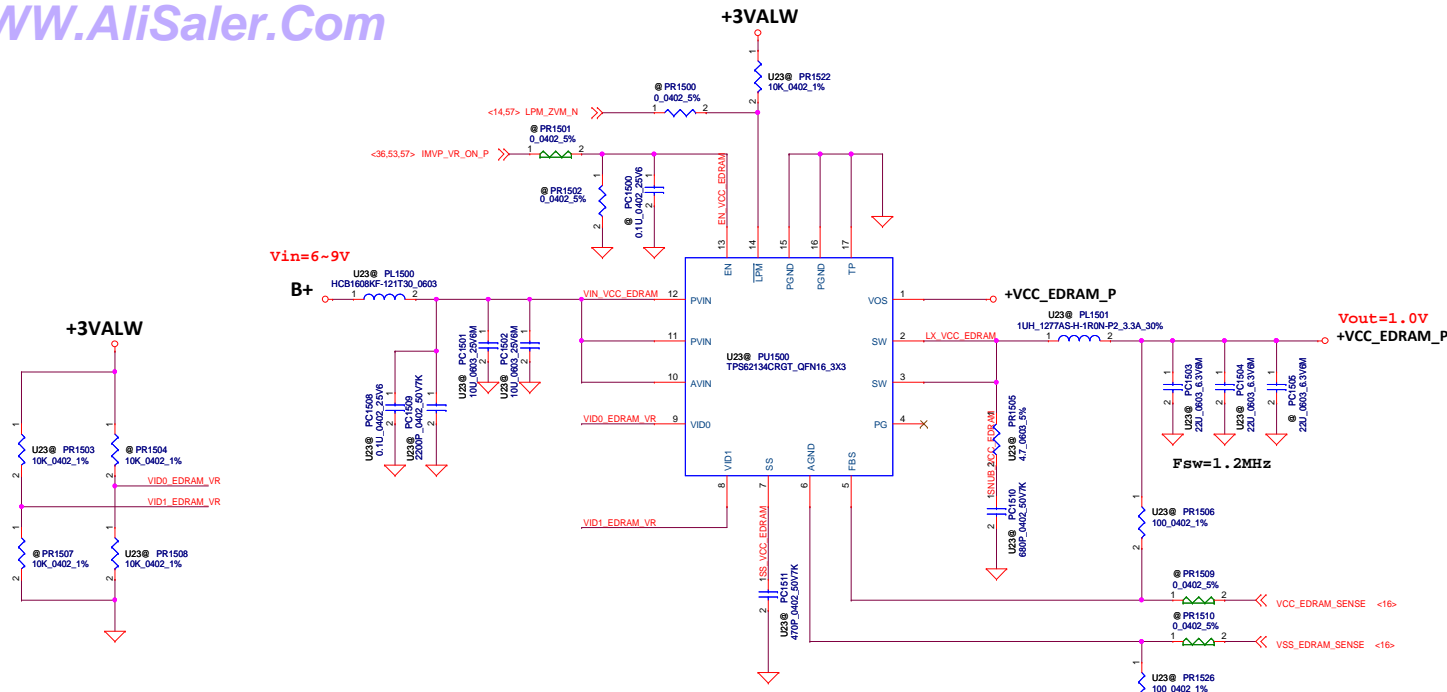
330u_B2*4 pcs



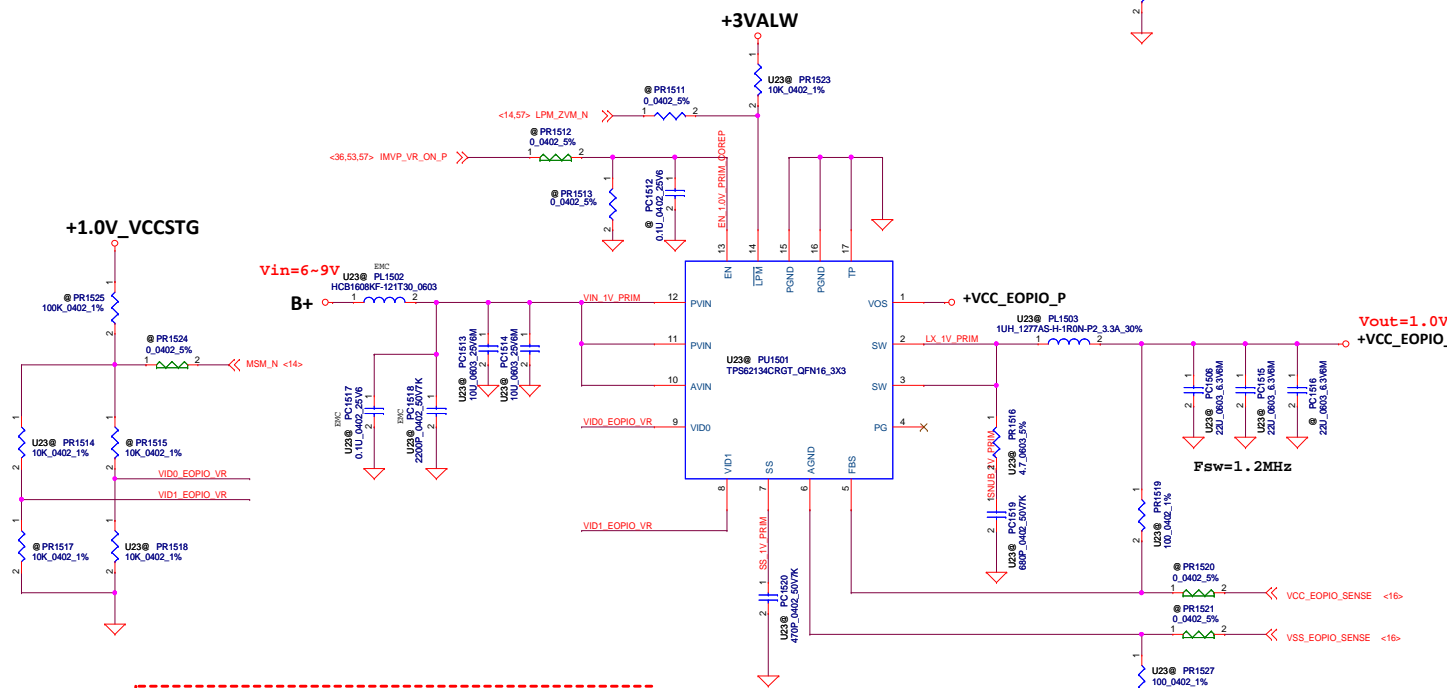
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	P55-PWR CPU BACK SIDE MLCC
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+VCC_EDRAM
TDC 1.75A
Peak Current 2.5 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm



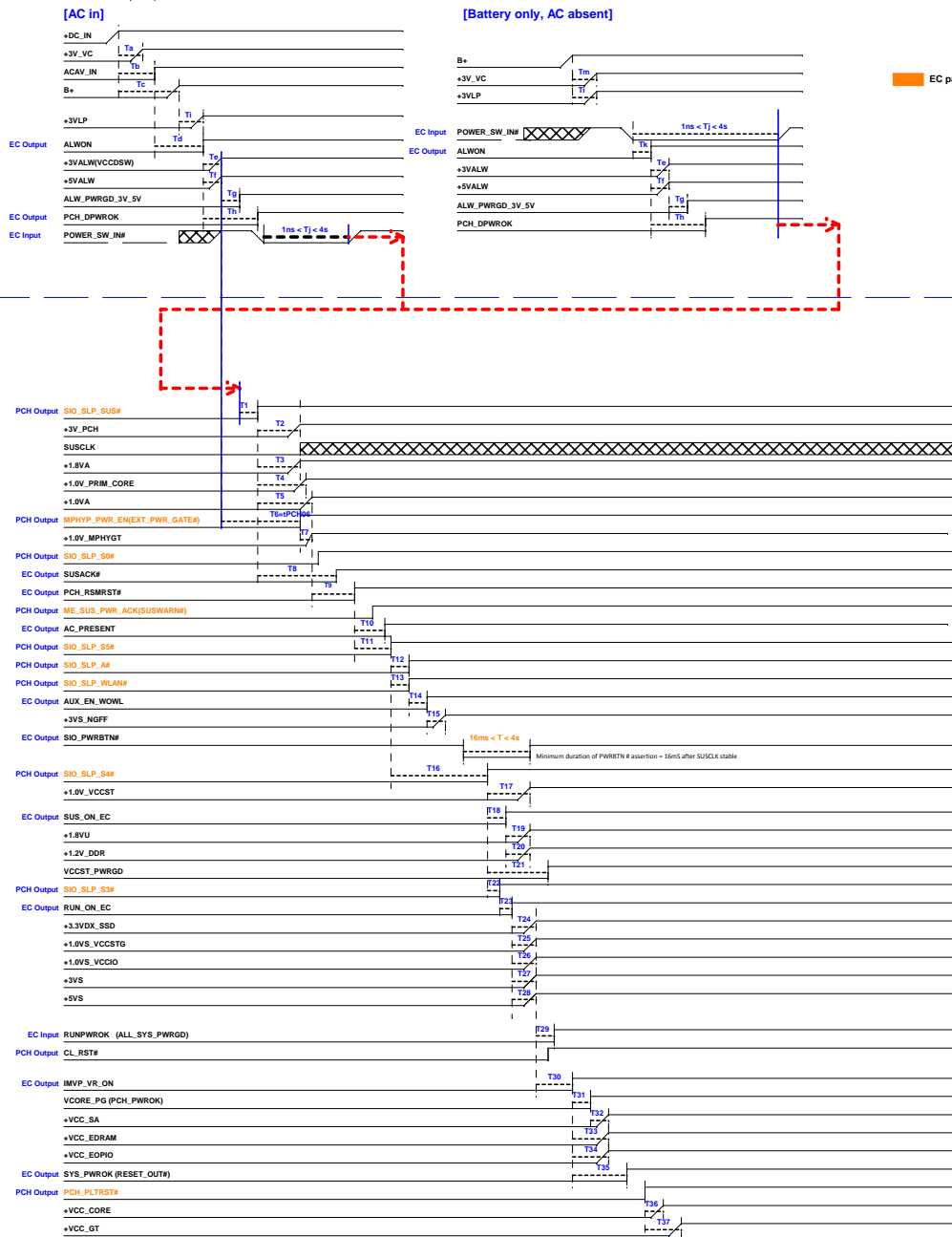
+VCC_EOPIO
TDC 1.4A
Peak Current 2.0 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

+VCC_EDRAM controller(35.25), Support component(35.26)
+VCC_EOPIO controller(35.27), Support component(35.28)

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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title
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Size				Document Number
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WARRANTY INFORMATION						Document Number
						LA-C881P
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Discrete Power On Sequence



[AC in]				[Battery only, AC absent]			
ITEM	Measure Point		Time	ITEM	Measure Point		Time
Ta	+DC_IN	To	+3V_VIC	Ta	ALWON	To	+3VALW
Tb	+DC_IN	Tb	+ACAV_IN	Tb	ALWON	Tb	+3VALW
Tc	+DC_IN	Tc	B+	Tc	ALWON	Tc	+3VALW
Td	ACAV_IN	Td	ALWON	Td	ALWON	Td	+3VALW
Te	ALWON	Te	+3VALW	Te	ALWON	Te	+3VALW
Tf	ALWON	Tf	+3VALW	Tf	ALWON	Tf	+3VALW
Tg	+3VALW	Tg	ALW_PWRGSD_3V_5V	Tg	+3VALW	Tg	ALW_PWRGSD_3V_5V
Th	ALWON	Th	PCH_DPWRGK	Th	ALWON	Th	PCH_DPWRGK
Ti	B+	Ti	+3VLP	Ti	B+	Ti	+3VLP
Tj	POWER_SW_in#	Tj	POWER_SW_in#	Tj	POWER_SW_in#	Tj	POWER_SW_in#
				Ym	B+		+3V_VIC

ITEM	Measure Point	Time
11	+3VALW	BD_SLP_SUS#
12	SDCSP_SUS#	HW_PSTH
13	SD_SLP_SUS#	+1WA
14	SD_SLP_SUS#	+10V_PRRM_CORE
15	SD_SLP_SUS#	+10V_PRRM
16	+3VALW	MPWP_PWR_EN
17	MPWP_PWR_EN	+10V_PRRMGT
18	SD_SLP_SUS#	SUS2OK#
19	+10VA	PCH_RSMRST#
110	PCH_RSMRST#	AC_PRESENT
111	PCH_RSMRST#	BD_SLP_S#
112	PCH_RSMRST#	BD_SLP_S#
113	SD_SLP_S#	BD_SLP_WLAN#
114	SD_SLP_WLAN#	AUX_EN_WOVL
115	AUX_EN_WOVL	+3VS_NGFF
116	SD_SLP_S#	BD_SLP_S#
117	SD_SLP_S#	+10V_VCCST
118	SD_SLP_S#	SUS_ON_EC
119	SUS_ON_EC	+18VU
120	SUS_ON_EC	+12V_DDR
121	SD_SLP_S#	SUS2_PWRBOD
122	SD_SLP_S#	BD_SLP_S#
123	SD_SLP_S#	RUN_ON_EC
124	RUN_ON_EC	+33VDC_SSD
125	RUN_ON_EC	+10VS_VCCST
126	RUN_ON_EC	+10VS_VCCD
127	RUN_ON_EC	+3VS
128	RUN_ON_EC	+5VS
129	+3VS	RUPWRKOK
130	MPWP_VR_ON	MPWP_VR_ON
131	MPWP_VR_ON	VCCORE_PG(PCH_PWRKOK)
132	VCCORE_PG(PCH_PWRKOK)	VCCO_S3A
133	MPWP_VR_ON	VVOC_EDRAM
134	MPWP_VR_ON	VVOC_EOPD
135	MPWP_VR_ON	RTS_PWRKOK(RESE_T_OUT#)
136	PCH_PRTSR#	VVOC_VCORE
137	PCH_PRTSR#	VVOC_VET